RWTH AACHEN UNIVERSITY

TECHNISCHE UNIVERSITÄT KAISERSLAUTERN

# Optimization of 100 Gb/s Short Range Wireless Transceivers under Processing-Energy Constraints

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# Agenda

- Motivation
- Proposed Approach
- Work Plan

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- **Motivation**

*Why processing energy as baseline?*

- **Proposed Approach**
- **Work Plan**

# Motivation

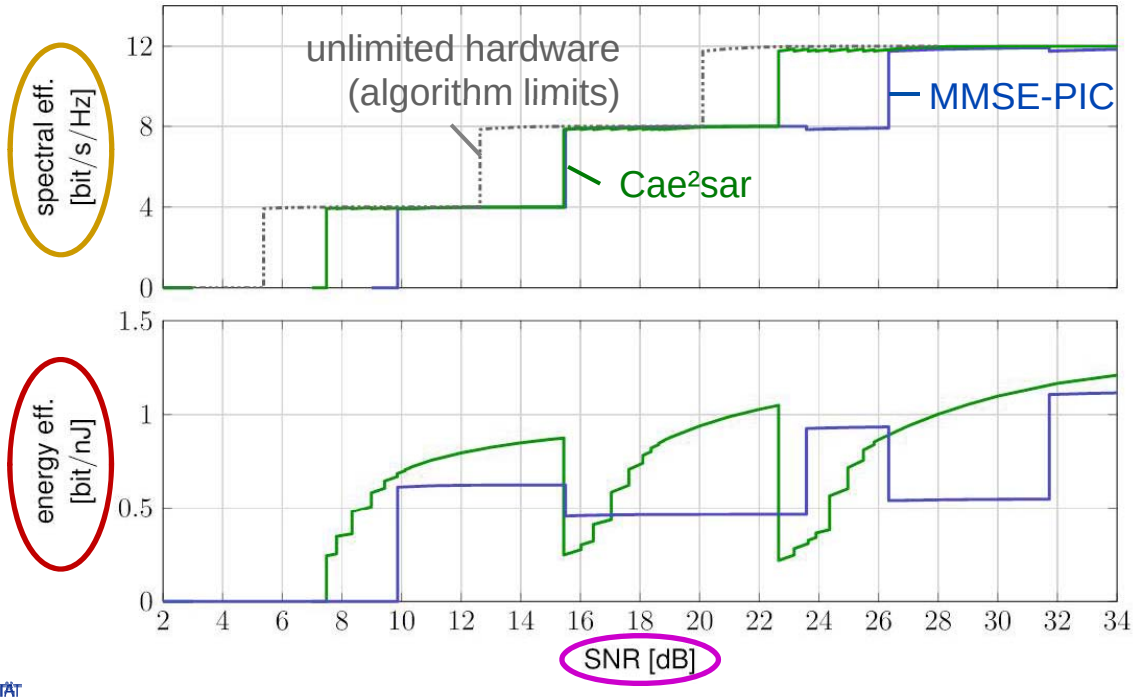
- **Power/energy consumption is critical**
  - Battery operation
  - Issue of heat dissipation (consumer packaging)
  - Increased temperature degrades performance (clock speed, variability)
  - Smaller technology nodes are more susceptible to temperature induced degradations

- **Assuming 1 W for processing in a 100 Gb/s transmission** (excluding transmit power)
  - Available energy per bit: 10pJ/bit
  - Required energy per MAC-operation (ITRS prediction):
    - 2.0 pJ @ 22 nm
    - 0.7 pJ @ 8 nm

# Motivation

- **There are three important boundaries in the design of a wireless transmission system:**
  - Power efficiency
  - Spectral efficiency
  - Implementation efficiency

**⇨ These efficiencies are not independent!**




**Example:**
First two SISO MIMO Demapper ASICs in the world
- MMSE-PIC: ETHZ
- Cae²sar: RWTH

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- **Proposed Approach**

*Design Space Exploration*

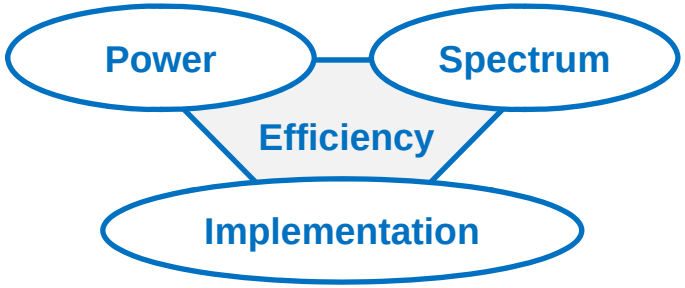
- Work Plan

# Research Goals

- **Basic spectral efficiency considerations:**
  - Assuming Nyquist rate transmission, 100 Gb/s requires
    - 50 GHz bandwidth for 2x1 bit/symbol (1 bit per I and Q)
    - 2x50 bit/symbol for 1 GHz bandwidth
- **3 Scenarios**
  1. Carrier frequencies below 10 GHz
     ⇨ available bandwidth per transmission in the order of 1 GHz
  2. Towards sub-mm and optical frequencies above 120 GHz
     ⇨ very large bandwidths available
  3. Intermediate frequency range, mainly around 60 GHz
     ⇨ several GHz of bandwidth available
- **Our research target:**
  - Phase 1: Scenario 3 ($f_c$ around 60 GHz)
    How many bit/symbol within processing energy constraints?
  - Phase 2: Continuation scenario 3 + scenario 2 ($f_c$ above 120 GHz)

# Research Approach

- **Design space exploration**
  - Algorithmic
    - modulation/coding
    - Beamforming/MIMO
  - Architectural
    - partitioning analog vs. digital
    - relaxing A/D-interface requirements




- **Prototyping of critical building blocks**
  - Hybrid implementation

# Example for Approach

- **Equalization**

  Analog filter (compared to digital filter):

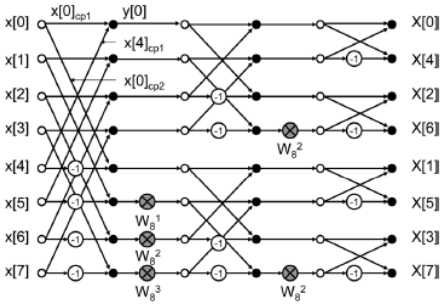
  + lower power consumption
  + high throughput
  + simpler A/D-interface
  - requires adjustable components
  - implementation tolerance and drifts

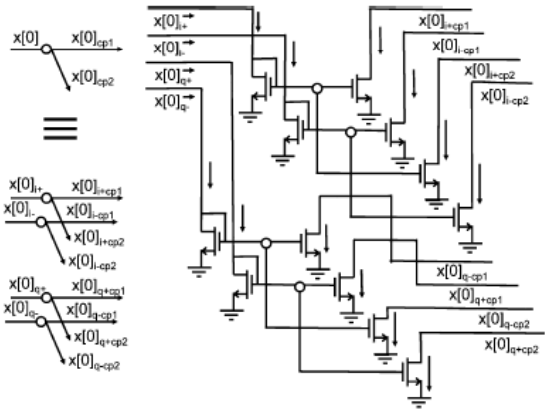
  ⇨digital compensation

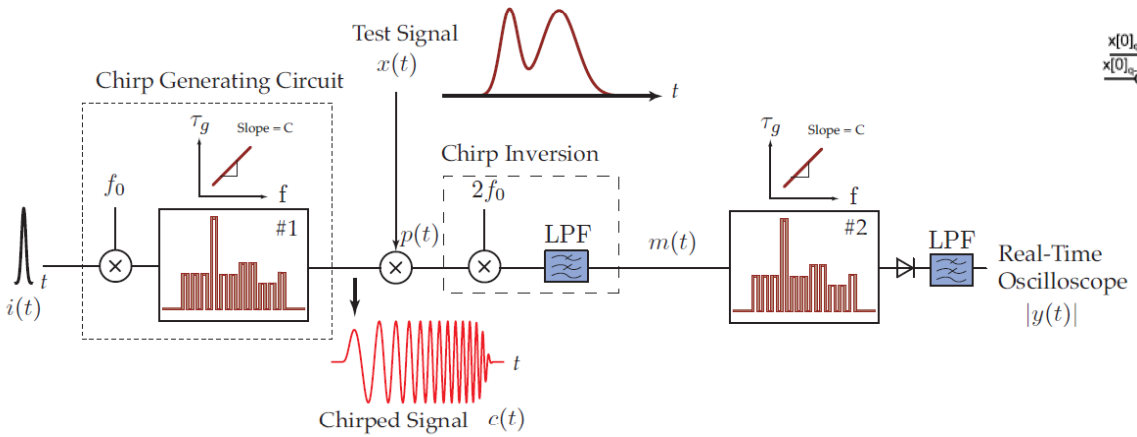
  ⇨digital control

# Example for Approach

- **Fast Fourier Transform**
  - Digital implementation
  - Analog implementation using active components*
  - Analog implementation using mainly passive components**






* Sadeghi, N.; Gaudet, V.; Schlegel, C.: „Analog DFT Processors for OFDM Receivers: Circuit Mismatch and System Performance Analysis“, IEEE Trans. on Circuits and Systems-I, vol. 56, no. 9, Sept. 2009, pp. 2123-2131.

** Gupta, S.; Caloz, C.:” Analog Real-Time Fourier Transformer using a Group Delay Engineered C-Section All-Pass Network”, IEEE Antennas and Propagation Society International Symposium 2010, pp. 1-4.

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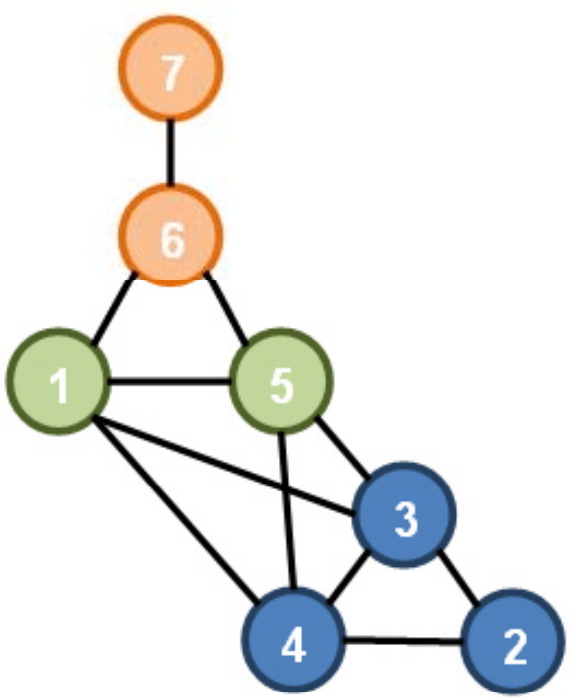
*Team Interaction*

# Dependencies between Work Packages




| WP # | Title |
|---|---|
| 1 | RF-architectures |
| 2 | Channel modeling |
| 3 | Modulation and coding |
| 4 | Beamforming/MIMO |
| 5 | Joint analog/digital signal processing architectures |
| 6 | Power estimation |
| 7 | Energy budgeting |

# Thank you
# for your attention !