- DataRace -

Fully Integrated Dual-Polarized Antenna Array with Ultra-Wideband Single-Chip CMOS Receiver

D. Maurath\textsuperscript{1}, S. Vehring\textsuperscript{2}, B. Deutschmann\textsuperscript{3}, M. Giese\textsuperscript{3}, A. F. Jacob\textsuperscript{3}, G. Böck\textsuperscript{2} and F. Gerfers\textsuperscript{1},

\textsuperscript{1}Technische Universität Berlin, Fachgebiet Mixed-Signal Circuit Design,
\textsuperscript{2}Technische Universität Berlin, Fachgebiet Mikrowellentechnik,
\textsuperscript{3}Technische Universität Hamburg-Harburg, Institut für Hochfrequenztechnik

friedel.gerfers@tu-berlin.de
datarace@msc.tu-berlin.de
Outline

1. Introduction

2. SPP 1655 – Project Results

3. SPP 1655/2 – Objectives

4. Conclusions and Outlook
Enabling Technologies for 100 Gb/s

- Low-cost system-in-package
  - Beam-forming system
  - 3D polymer-integrated antenna array
  - Single-chip CMOS transceiver

- Targeting mass-market applications
  - Office-space short-range link (up to 1 m)
  - Video-streaming in airport departure lounges

- Take advantage of entire W-band (75-110 GHz)
  - High relative bandwidth
  - Moderate modulation complexity (moderate SNR)
Array-based Communication Systems

- Arrays for
  - Free space power combining
  - System scalability
  - 2D Phased arrays / beam steering

- Circular polarization
  - Antenna alignment uncritical

- Dual polarization
  - Double data rate
  - Relaxed link budget requirements
Low-Cost Technologies I

- Polymer process:
  - Vertical growth by polymer deposition and UV-curing
  - Inclined metalized walls
  - Fine resolution (µm scale)
  - Reliable interconnects

- Antenna-in-package
  - Small chip area even for arrays
  - Improved performance
  - Moderate area consumption
  - Wideband system-in-package up to W-band

Antenna packaging:
- CM: Conventional module
- AiP: Antenna-in-package
- AoC: Antenna-on-chip

[Tripodi et al.]
Arrays: Brick vs. Tile

- **Brick**
  - Simple RF interconnects
  - Scalable to high frequencies
  - Compatible with waveguide

- **Tile**
  - Layered arrangement
    - Multi-layer PCB process
  - Low thickness
Low-Cost Technologies II

- CMOS technology
  - Highest integration density
  - Mixed signal SoC
  - High reliability
  - Cheap mass production

- CMOS gate length downscaling leads to
  - Increasing fT/fmax
  - Lower current consumption
  - Downscaling driven by digital computing
    - Highest integration density
    - Cheap mass production

60 GHz CMOS PA with 0.27 mm² chip area
Low-Cost Technologies III

- Nanometer CMOS provides ultra wideband devices ($f_{max}$ & $f_T$)
- But, we can’t build circuits with intrinsic transistors!
- Impact of BEOL parasitics worse in CMOS than SiGe! (2-3 Generations)
SiGe (IBM) $f_T$
NFET $f_T$ for nm CMOS Processes
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Overall TX Front-End – An Overview

Topologies:

**Topology 1**
- Inline transition for true brick
- Septum polarizer for compactness

**Topology 2**
- Vertical transition for dual polarization
- Dielectric plate polarizer for simple setup
Overall TX Front-End - Transition

- 50 Gbit/s... CMOS PA Flip-Chip
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- Transition
  - μ-strip
  - WR10
- Polarizer
  - + Horn Antenna

Topology 1
- Inline transition for true brick
- Septum polarizer for compactness
Active Antenna Array for Transmission

- 3D polymer-metal process
- Production of two demonstrators (topology 1 and 2)
W-Band Power Amplifier Design

- Challenge → Achieve Pout and PAE over 38% relative bandwidth

- Features
  - 40 nm CMOS technology, fully differential 4-stage design, neutralized transistors, transformer coupling, broadband matching
W-Band Power Amplifier Design - Results

Results
- 18 dB small signal gain
- $P_{out} > 10$ dBm
- PAE $> 10\%$
- 38\% relative bandwidth
- Good correlation sim/meas.
Comparison with state-of-the-art - FOM

![Graph showing comparison between E-Band and This work in terms of Pout·PAE and Bandwidth as a percentage. E-Band has a higher Pout·PAE for a given Bandwidth compared to This work.]
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Receiver System

- CMOS chip integration in dual-polarized horn antenna
  - Using 3D polymer-metal process
  - System-in-Package

75-110 GHz
Receiver System

- Single-chip, dual-channel RF-to-digital conversion
- 28 nm high-K metal gate (HPC) CMOS technology
- Full bandwidth low-IF concept (1-36 GHz), no IQ-splitting
Receiver System

- Single-chip, dual-channel RF-to-digital conversion
- 28 nm high-K metal gate (HPC) CMOS technology
- Full bandwidth low-IF concept (1-36 GHz), no IQ-splitting
Receiver System

- External LO / clock generation (18 GHz LO to link tests)
  - Two on-chip frequency doubler to 74 GHz
- Beam steering
  - Digital phase shifters
Receiver System

- Power combining at IF
  - Pro: simple
  - Con: channel interference and SNR
**Receiver System**

- Impedance-conversion to drive 74 GS/s T&H
- 74 GS/s (time-interleaved) ADC
- 5 bit ENOB
- RF-to-Digital outputs (decimated output or on-chip memory)
Receiver-Topology - Power Combiner

Wilkinson power combiner
- Limited bandwidth
  - Multiple sections
- Lumped element resistor needed
  - Film-resistors with less parasitics

3-Steps

5-Steps

Losses vs. Bandwidth
Multi-layer feed network
- Monolithic integration
- 3D polymer-metal process
- LO distribution network and ADC on separate motherboard
Receiver-Topology - Antenna Array II

- Feed network in line w/ front-end
- Antenna rows
- Grown layer-wise
- Interconnected on motherboard
- Land- or ball-grid for 2nd level interconnects
- Tile architecture for feed network
- Vertical growth
- Integrated layer interconnect
- Full monolithic 3D integration
Receiver-Topology - RF-to-IF Converter

- Single-chip dual-channel receiver

![Diagram of RF-to-IF converter]

- RF$_{in}$ pol1
- RF$_{in}$ pol2
- LO pol1,2
- IF$_{out}$ pol1
- IF$_{out}$ pol2
- Dig$_{out}$ pol1
- Dig$_{out}$ pol2

**Components:**
- LNA
- MIX
- BBA
- ADC
- IF-to-digital converter

**Note:**
- RF-to-IF converter
- Single-chip dual-channel receiver
Receiver-Topology - RF-to-IF Converter

- Single-chip dual-channel receiver

**RF-receiver modules**
- 28 nm CMOS
- Low-noise amplifier
- Down-conversion mixer
- Baseband amplifier (BBA)
- LO quadrupler 18 to 74 GHz

**Features/Objectives**
- Full W-band operation
- NF < 7 dB
- Analog gain > 55 dB
- BBA = 1 – 36 GHz (190% BW)
- Output power > 0 dBm

- Design challenge: baseband amplifier with 190% bandwidth!
Baseband Amplifier 1 – 36 GHz

- How to achieve high gain with 190% relative bandwidth?

- Classic distributed amplifier (DA)
  - Pro: Inherently broadband
  - Con: low gain
Baseband Amplifier 1 – 36 GHz

- How to achieve high gain with 190% relative bandwidth?

- Solution
  - Re-use forward and backward gain of DA
  - Multi-stage: combining 3 DA stages \( \Rightarrow \sim G^5 \)
Ultra-wideband (74GS/s) digitizer (direct UWB IF-to-digital conversion)

>350Gbit/s effective RX resolution enabling simple modulation schemes (BPSK, QPSK) as well as channel equalization (offline)
UWB IF-to-Digital Conversion – Overview

- Time-interleaved T&H & ADCs
- Impedance-conversion to drive T&H
- 40GHz T&H bandwidth with 6bit ENOB
CMOS 28nm Technology Test

- $R_{on} = 10\text{-}40 \Omega$
- $f_{T,n}(TT) = 120 \text{ GHz}$
- $C_{min} (kT/C) = 50 \text{ fF}$
- Challenge: switch performance limitation due to $C_{GS}$ & $C_{DS}$

SNDR = 45.1 dB $\Rightarrow$ 7.2 bit ENOB

SNDR = 45.1 dB

-13.4 dB signal
-58.5 dB spurs

FFT signal out (dB)

frequency (GHz)

0
1
20

SNDR $\Rightarrow$ 7.2 bit ENOB

ADC

clk

IF(t)

IF(nTS)

X

Y
Time-Interleaved ADC

- Time-Interleaved ADC uses many parallel ADC channels operating at a lower speed (comparable with multiple CPU cores)
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- Digital gain and offset mismatch calibration
- Mixed-signal timing mismatch calibration
100 Gb/s System Demonstrator

- CW system performance (TUHH anechoic chamber)

- Digital data communication
  - (Univ. Duisburg-Essen, SPP 1655/2 - Tera50+, Prof. Stöhr)

2 Options
- Analog IF outputs
- Digital outputs

System-level demonstration of 100 Gb/s W-band communication with digital beam steering
Collaboration Concept

- SPP 1655

- Interface and System Definition
  - RF Chip Components
  - ADC Chip Components
  - Univ. Duis.-Essen, Prof. Stöhr, Tera50+
  - Interface and Equipment

- Antenna Array Design
  - 3D System Integration
  - System Demonstration

- TUB
- TUHH
- Common Task
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Conclusions and Outlook

- **First project phase:** fully integrated low-cost transmitter with
  - CMOS BBPA and antenna array
  - dual circular polarization
  - system integration: work in progress

- **Second project phase:** fully integrated low-cost receiver with
  - single-chip receiver: LNA, BBA, down- and D/A-conversion
  - phased array with phase shifting LO
  - dual-polarization and independent steering
  - full-scale array and system demonstration
Thank you for your attention