Strategies for Energy-Efficient 100 Gb/s Baseband Processing Using Mixed Analog/Digital Signal Processing

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Outline

- Options for 100 Gb/s wireless
- Considerations wrt. a 100 Gb/s digital BB
- Research directions for a 100 Gb/s mixed-mode BB processor
- Conclusions

Options for 100 Gb/s Wireless?

- **Extreme Spectral Efficiency (SE) x „moderate“ bandwidth (BW)**
  e.g. 10 b/sHz * 10 GHz
  → RF bands at 60 GHz, E-band

- **Moderate SE x extreme BW**
  e.g 4 b/sHz * 25 GHz
  → RF bands > 200 GHz

- **Free-space optics**
  e.g. 40 Gbaud with 8-PAM (3 b/sHz * 30 GHz)

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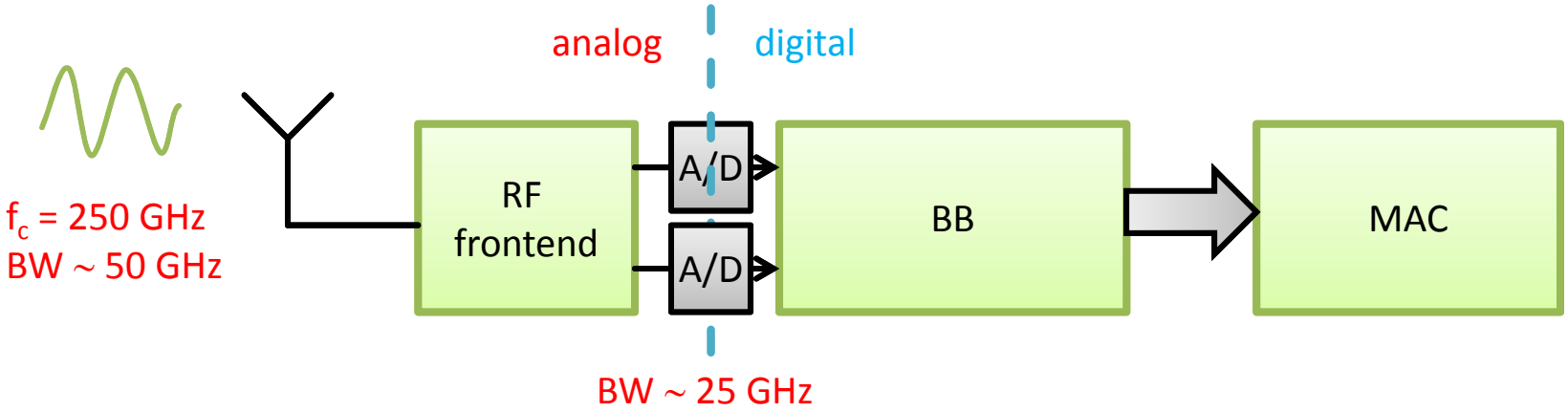
Our focus

- **Free-space optics**
  e.g. 40 Gbaud with 8-PAM (3 b/sHz * 30 GHz)

A Generic 100 Gb/s Receiver



- Receiver characteristics
  - f_c > 200 GHz, *RF BW* ~ 50 GHz
  - *SE* 3b/sHz
  - *BB BW* ~ 25 GHz

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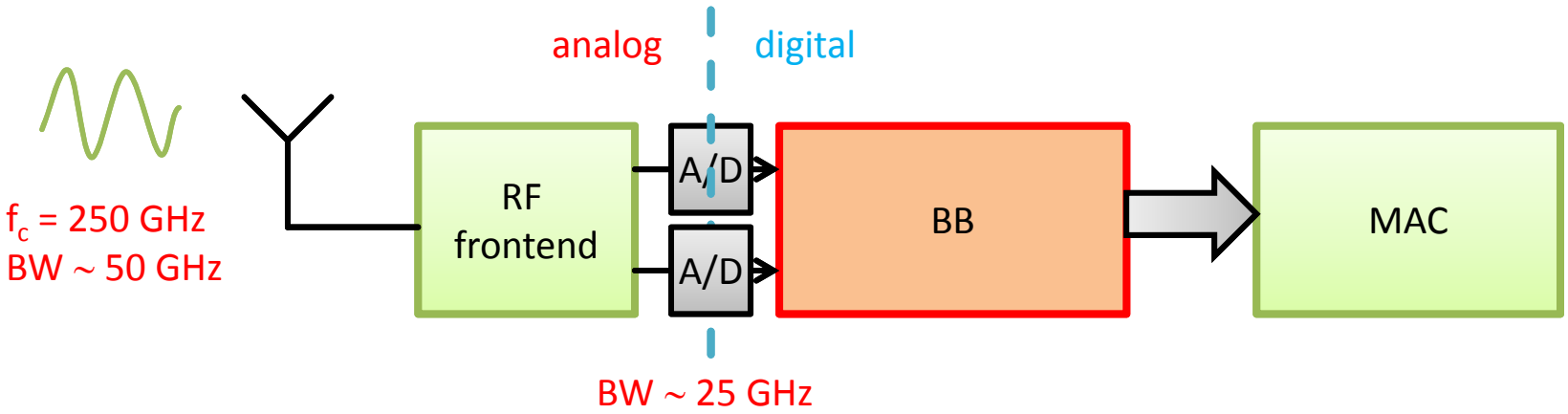

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Is the BB feasible from HW perspective?

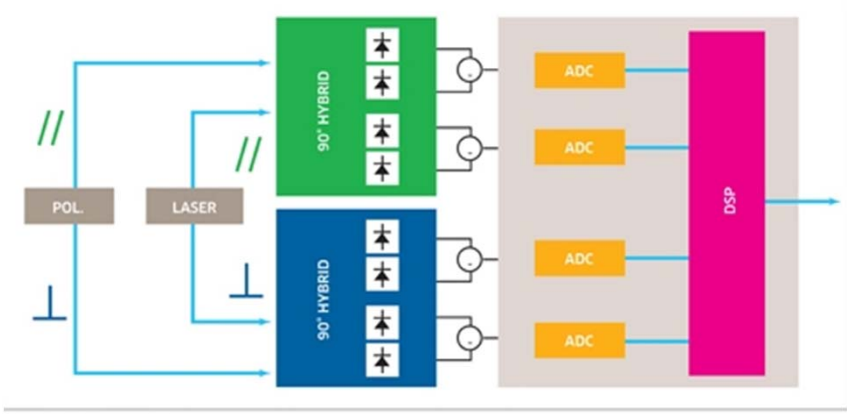
How to implement it?

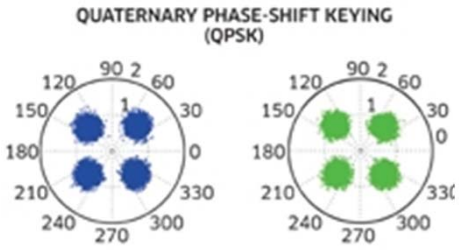
100 Gb/s Digital BB …

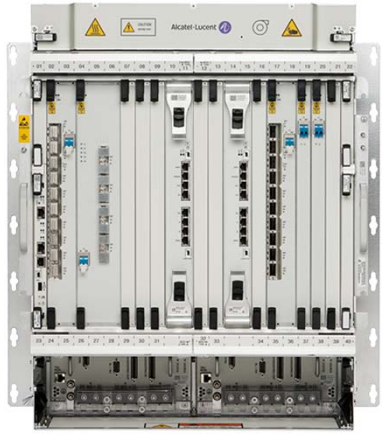
… is already there!

- 100 GbE fiber-optic products out since 2013

- Use extensively wireless technology
  - Optical QPSK, 28 Gbaud, polarisation MUXed
  - Coherent detection, DACs, ADCs, fully digital baseband
  - Carrier recovery, synchronization, equalization, error correction







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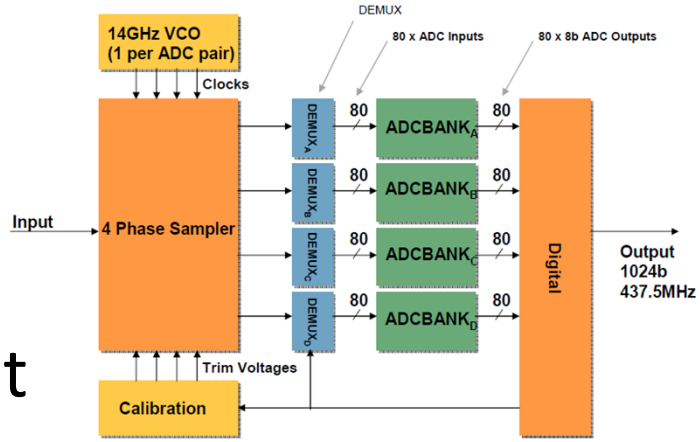
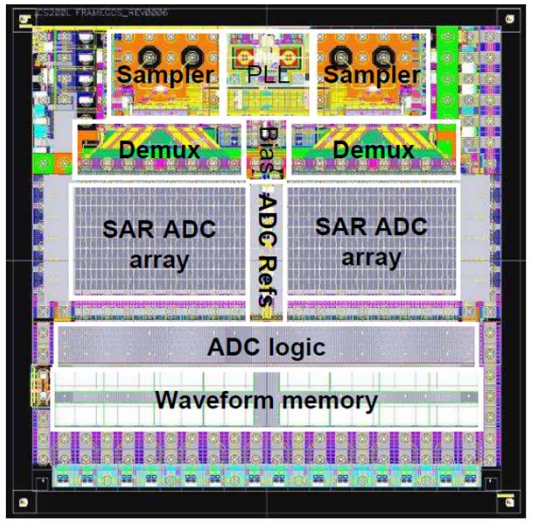
56 GS/s 8 Bit ADC[1]

- 320 time-interleaved SAR ADCs
- A Single SAR ADC with
  - 175 MS/s, 8 bit
- Analog BW 16 GHz, ENOB >5.7 bit
- Power dissipation <2W (!)
- Design by Fujitsu Europe
- 65 nm CMOS

→ ADCs are feasible. Power will benefit from further CMOS scaling.



56 GS/s ADC Block Diagram



Dual-56 GS/s ADC test chip

[1] **Ian Dedic „56 GSps ADC Enabling 100GbE“, OFC 2010**

100 Gb/s Digital BB …

- In fiber-optic 100 GbE receiver DSP performs carrier recovery, synchronisation, channel equalization, error correction on 2*28 Gbaud 6-8 bit data
- DSP needs ~30 TOPS[1]
- Power target 4 ADCs + DSP ~50 W [1]

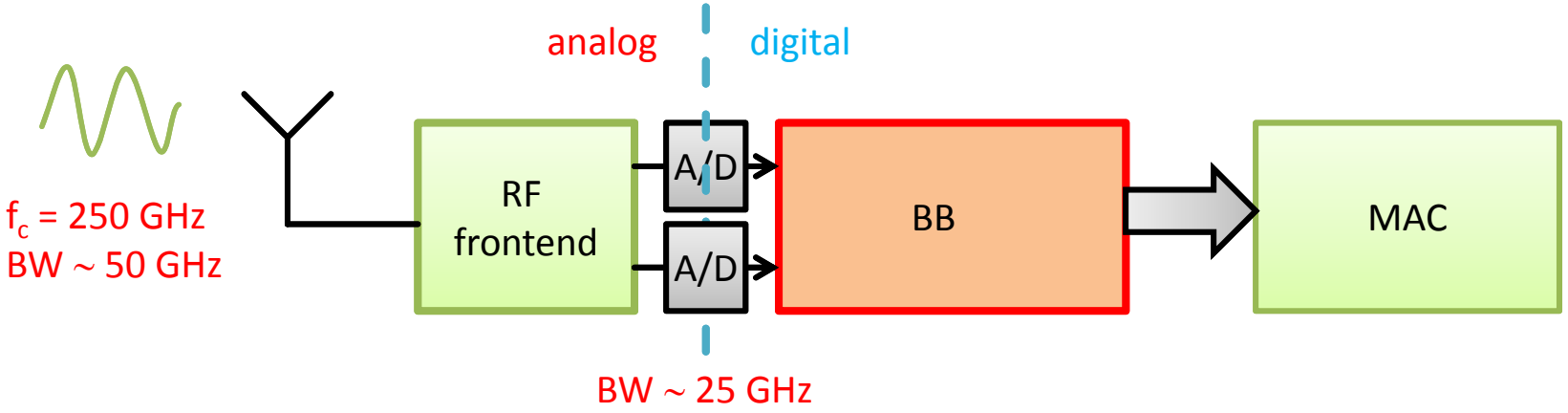
→DSP dominates BB power dissipation in 100 GbE.

→Could be true for wireless 100 Gb/s, too.

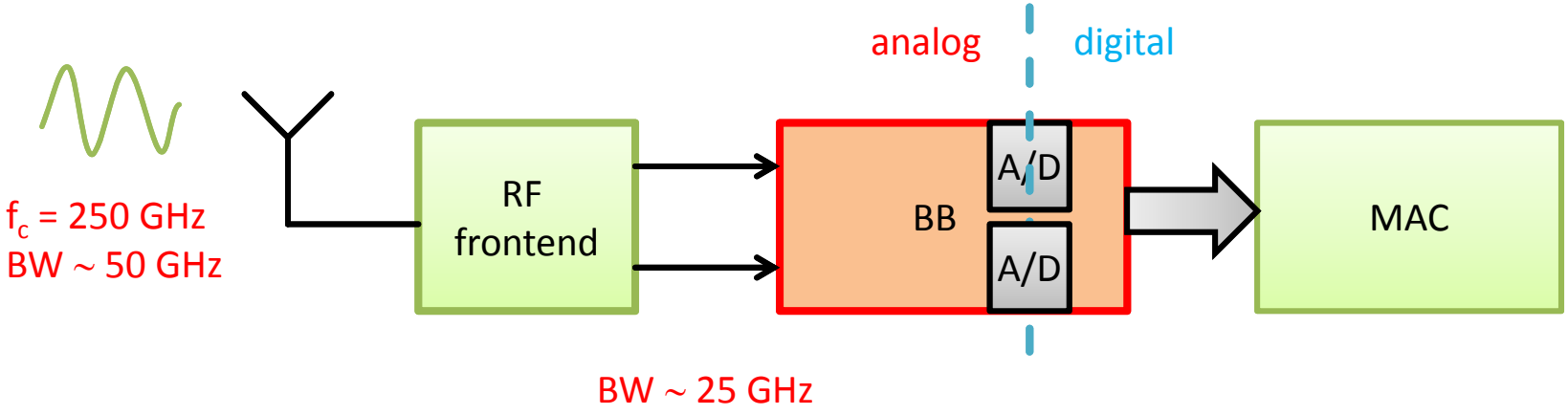
(„Disclaimer“: CMOS Scaling will help, equalization will be simpler for short range wireless links, only moderate spectral efficiency considered. → research topic)

[1] Ian Dedic „56 GSps ADC Enabling 100GbE“, OFC 2010

Research Approach

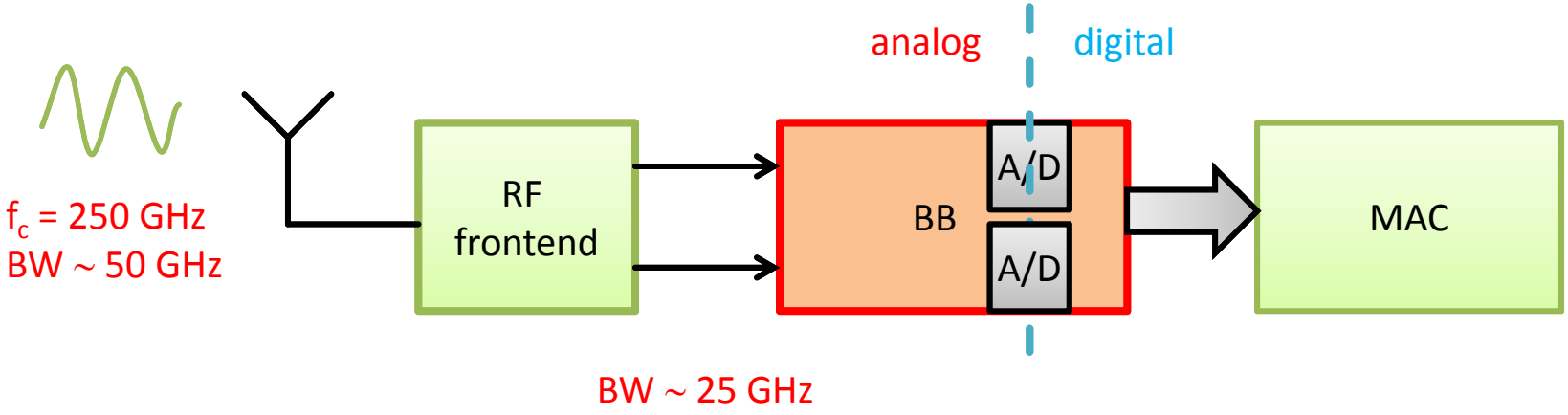


Research Approach



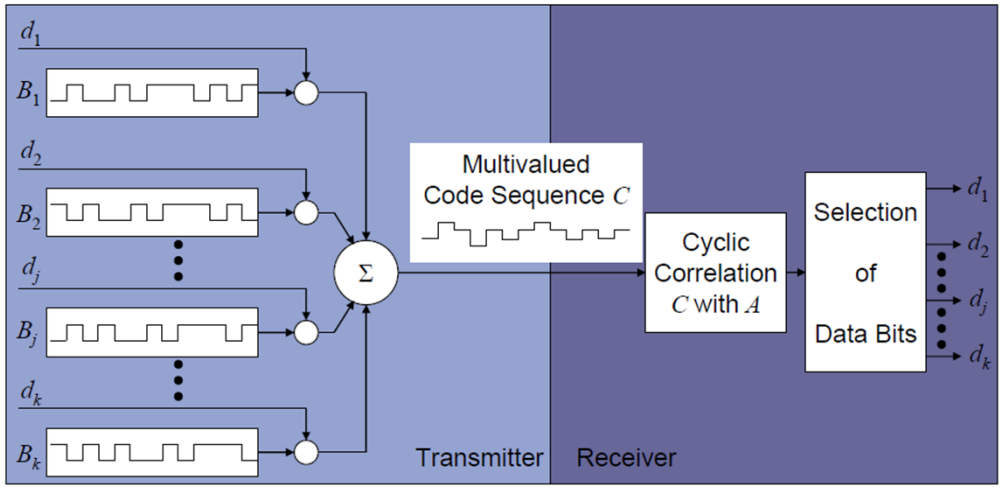
Shift „analog boundary“ → Mixed-mode BB w. dominant analog

Research Approach



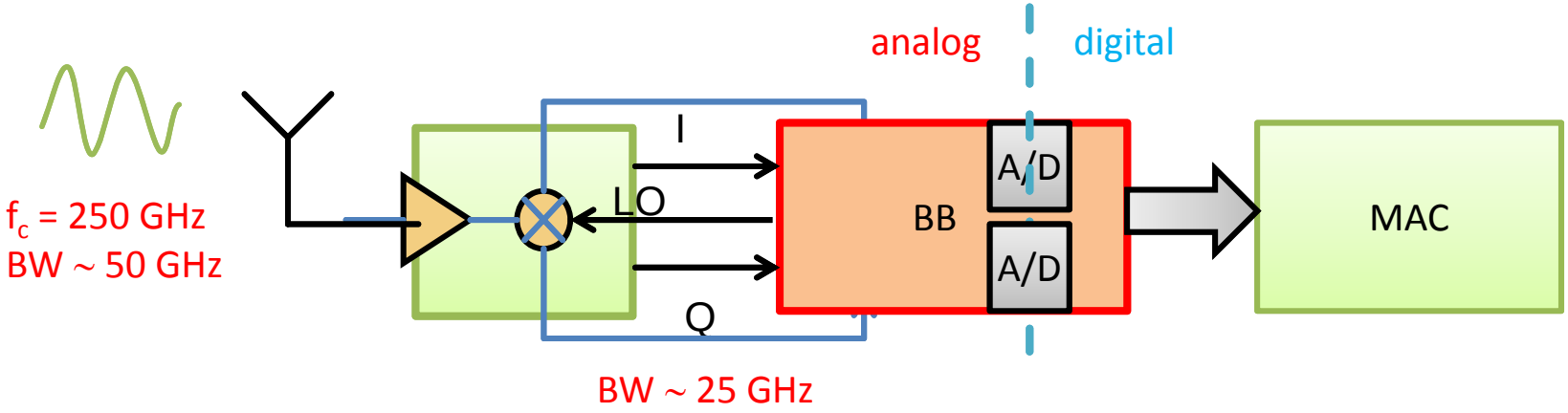
- **Analog processing** → hardware-efficient, (potentially) power-efficient
- **Choose „Analog-friendly“ modulation & coding** → Parallel Spread-Spectrum Sequencing (PSSS) simplifies mixed-mode BB implementation
- **Sync. Detection at RF** → Comes at little extra hardware / power effort
- **Preprocessing in analog domain** → reduced dynamic range for ADCs, smaller DSP

Parallel-Spread-Spectrum Sequencing (PSSS)



- Known coding technique from IEEE 802.15.4-2006
- Transmitter: k symbols (d_1 to d_k) are spreaded by orthogonal codes B_1 to B_k and summed before transmission.
- Receiver: The k symbols are retrieved by means of cyclic correlation.
- **PSSS is „analog-friendly“, simplifies mixed-signal coding and equalization.**

Synchronous Detection at RF



- Digital carrier recovery and synchronisation at 100 Gb/s will be power-hungry.
- **Synchronous detection in RF domain comes at little extra hardware effort and power.**

Conclusions

- 100 Gb/s with moderate SE requires f_c well beyond 100 or 200 GHz and extreme BB bandwidth.
- ADCs and digital BB are clearly feasible but DSP power likely to be excessive for mobile applications.
- Mixed-mode BB with dominant analog will reduce hardware effort (certainly) and power dissipation (potentially).
- PSSS as an „analog-friendly“ coding / equalization scheme.
- Synchronous detection at RF as efficient alternative to digital carrier recovery / synchronisation.