# Low-Power System Architectures for Future 100GBit/s Wireless Communication Systems

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## 100 Gbit/s Transceivers: Challenges / Motivation

- Very high carrier frequency and/or high order modulation schemes required
  e.g. $f_c$ = 250 GHz, 16 QAM with 25 Gbaud/s

- Currently available semiconductor technology limited
  e.g. to $f_T$ / $f_{MAX}$ < 300/500 GHz

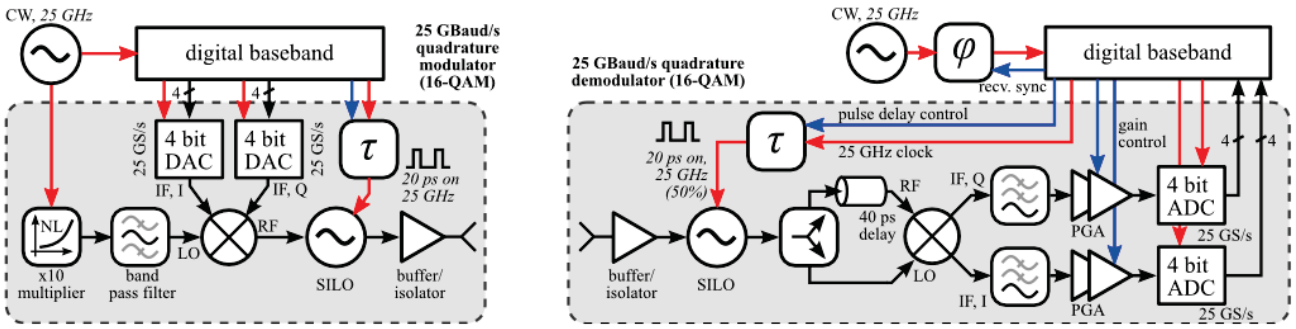
→ very limited gain in LNA and PA stages (typical $G$ < 6 dB)
→ long amplifier chains with stability and power consumption issues
→ poor noise figure
→ realization of circuits / systems with high dynamic range difficult

"Simple" scaling of existing heterodyne transceiver architectures is challenging and possibly not productive with given / future technology

**Stimulus for investigation of novel transceiver concepts**
**→ Stimulus for our proposed project**

# SPARS Transceiver – A Novel Transceiver Concept

- Central innovation under investigation: **SPARS transceiver concept**
  SPARS = Simultaneous Phase and Amplitude Regenerative Sampling




**Expected benefits of novel SPARS approach:**

- ≥ 40 dB signal boost in a single stage (Rx and Tx) @ 250 GHz expected (vs. << 6 dB gain in conventional approaches)
- No continuously running PLL, stabilized LO and no complex LNA / PA required
- Especially suited for self-mixing delay-hopped transmitted reference approach
- Regenerative Sampling Oscillator (SILO) inherently causes amplitude alignment
  → pre- and subsequent stages with moderate dynamic range sufficient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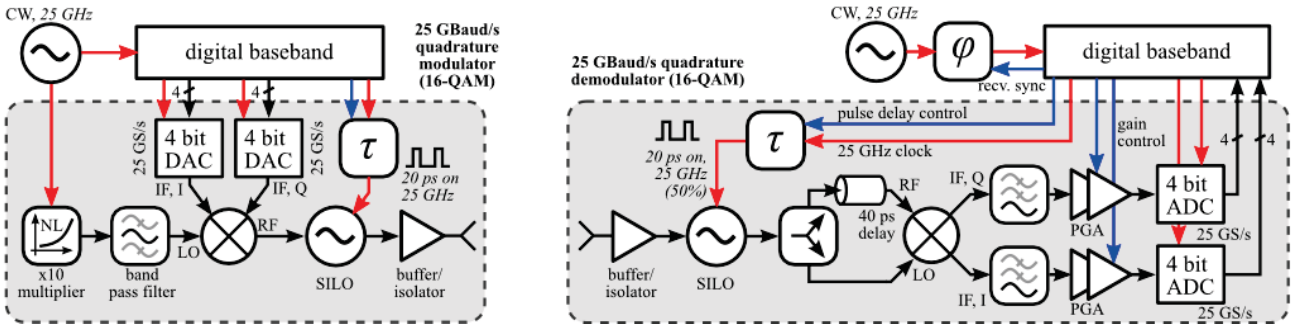



**Overall project goal:**

Overcome scaling and power dissipation issues by:

- Investigation / design of novel transceiver architecture
- Investigation / design of optimized required components
- Proof of concept by worldwide first 250 GHz SPARS transceiver demonstrator

# Preliminary Work

- ✓ Basic feasibility of SPARS transceiver demonstrated @ 5.8 GHz
  - *C. Carlowitz, A. Esswein,* ***R. Weigel and M. Vossiek****, "Regenerative Sampling Self-Mixing Receiver: A Novel Concept for Low Complexity Phase Demodulation "- to be published at IEEE International Microwave Symp., June 2013*
    **(selected as finalist for best paper competition)**
- ✓ Regenerative phase sampling of UWB and mm-wave radar signals
  - *Esswein, C. Carlowitz, G. Fischer,* ***M. Vossiek, R. Weigel*** *and T. Ussmüller, "An Integrated Switched Injection-Locked Oscillator for Pulsed Angle Modulated Ultra Wideband Communication and Radar Systems," in Proceedings of the IEEE International Conference on Ultra-Wideband, ICUWB 2012, Syracuse, USA, Sept. 2012.* **(best paper award)**
  - *Strobel, A.;* ***Ellinger, F.****; , "An active pulsed reflector circuit for FMCW radar application based on the switched injection-locked oscillator principle," Semiconductor Conference Dresden (SCD), 2011 , vol., no., pp.1-4, 27-28 Sept. 2011*
  - *C. Carlowitz, A. Strobel, T. Schäfer,* ***F. Ellinger and M. Vossiek****, "A mm-Wave RFID System With Locatable Active Backscatter Tag," IEEE International Conference on Wireless Information Technology and Systems 2012, Maui, Hawaii, USA, Nov. 2012.*
- ✓ Leading edge competence for high data rate and mm-wave system & chip design
  - *M. Grözing, F. Lang, T. Alpert, Hao Huang, D. Ferenci,* ***M. Berroth****, „25 GS/s 6 bit CMOS DACs and ADCs for 100Gbit/s Photonic networks", ITG-Fachbericht, ISBN 978-3-8007-3346-0, pp. 37-44.*
  - *M. Grözing, B. Philipp, M. Neher,* ***M. Berroth****, "Sampling Receive Equalizer with Bit-Rate Flexible Operation up to 10 Gbit/s", European Solid-State Circuits Conference (ESSCIRC), September 2006, pp. 16-19.*
  - ***F. Ellinger****, U. Jörges and S. Hauptmann, "Small signal analysis of quadrature LC oscillator operating at 59-62.5 GHz," IET Circuits, Devices & Systems, vol. 3, no. 6, pp. 322-330, December 2009.*
  - *I. Nasr, M. Dudek,* ***R. Weigel, and D. Kissinger****, "A 33% tuning range high output power V-band superharmonic coupled quadrature VCO in SiGe technology," in IEEE Radio Frequency Integrated Circuits Symposium, Montreal, Canada, pp. 301-304, June 2012.*

# Project Subtasks and Goals

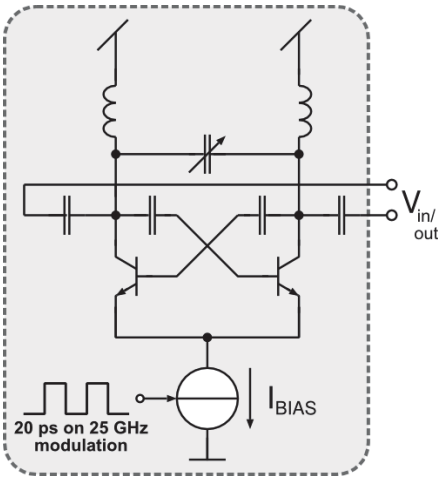
## 250 GHz SPARS Receiver Frontend Design

### State of the Art:

- Long chains of energy inefficient amplifiers

### Project goals:

- Pulsed regenerative sampling circuit up to 250 GHz
- Output power at least 40 dB above power of sampled signal in a single stage; high sensitivity of phase and amplitude sampling
- 16-QAM, 25 GHz switching frequency
- For the first time: fully integrated selfmixing demodulator at 250 GHz
- Operating close to technology limits → use of fastest BiCMOS technology with $f_{MAX} \geq 500$ GHz
- Development of analytical models for rigorous RFIC optimization



# Project Subtasks and Goals

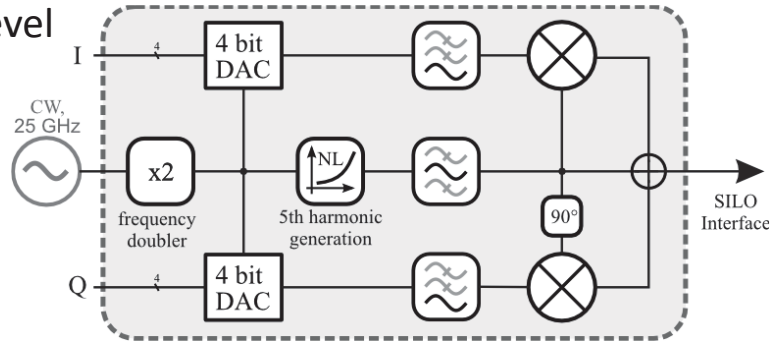
## 250 GHz Quadrature Modulator and High Speed DAC Design

**State of the Art:**

- High amplitude swing, high power consumption DACs and synthesizers

**Project goals:**

- Efficient, novel low power level 25 GS/s DAC and mm-wave modulator
- integrated antenna design
- LO up-conversion with frequency multiplier
- 250 GHz IQ modulator
- segmented RZ DAC exploiting relaxed power level requirements due to SPARS concept





# Project Subtasks and Goals

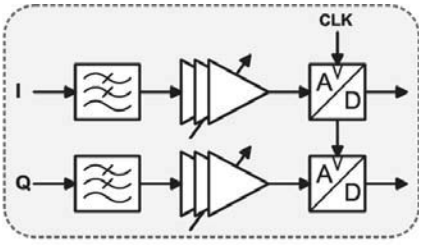

## 25 GS/s Receiver Analog Baseband Architectures and Design

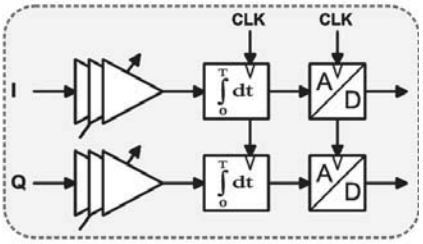
**State of the Art:**

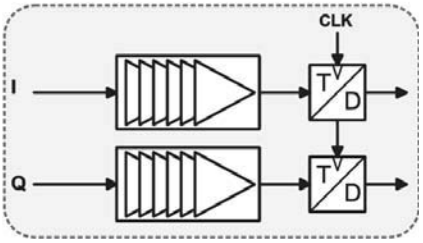
- only "conventional" receiver baseband approaches

**Project goals:**

- Investigate and implement alternative baseband concepts
- Integrator with 25 GHz reset, ADC → no ISI due to reset
- Limiting Amplifier + Time-to-Digital-Converter
- Special challenges and objectives:
  - pulsed baseband
  - optimizing for low power consumption



# Project Subtasks and Goals

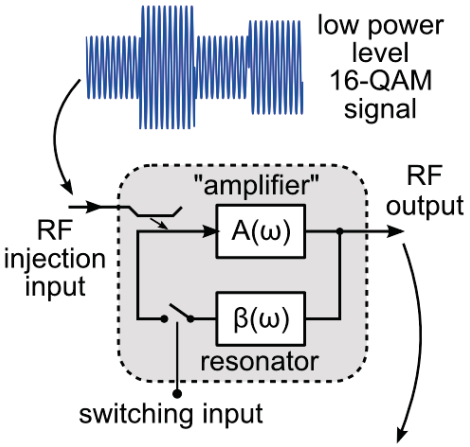
**System Concept Investigation and Experimental Verification**

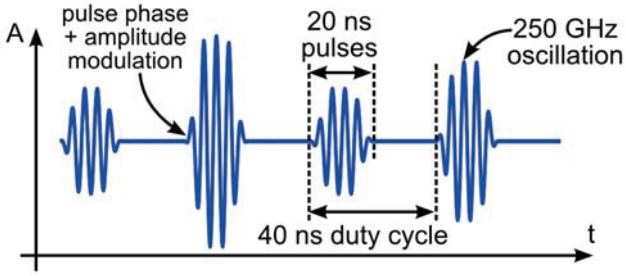
**State of the Art:**

- Heterodyne or superregenerative transceiver

**Project goals:**

- Verify and establish SPARS transceiver concept
- Analytic modeling and simulation considering technology limitations
- Error source analysis (noise, nonlinear distortions, spurs, ...)
- Experimental verification of developed theories and designs
  step 1: scaled demonstrator @ 30 GHz
  → faster knowledge acquisition
  → input for final system & RFIC design
  step 2: final 250 GHz demonstrator




# End of Talk

# Thank you for your attention