Front-Ends for High-Speed Mobile Data Communications at W-Band

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Outline

Why 100 GBit/s?

… one may ask.

- History has shown that users **will eventually use** the available bandwidth.

- Application scenarios:
  - Fast data transmission between devices (e.g., HDD to TV)
  - Seamless availability of cloud-stored data
  - Providing *many* users with a high data rate, i.e. >1 GBit/s (e.g., in departure lounges or shared offices)

Partners and Tasks

TU Berlin (BO 1520/7-1):
- CMOS power amplifier RFIC
- Efficiency, bandwidth

TU Hamburg-Harburg (JA 605/10-1):
- Integrated active antenna array
- Polarization multiplexing

Broadband front-end for W-band operation

System-in-package with CMOS PA and antenna array

Possible application

Multi-user short range LOS communication

Outline

1. Introduction

2. **Project Goals**

3. State of the Art and Novel Concepts

4. System Budget

5. Conclusions

Frequency Band of Operation

W-Band (75 – 110 GHz)

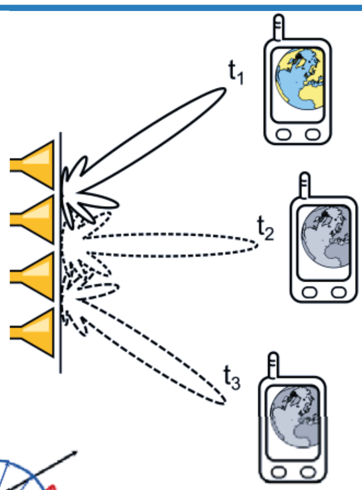
- 35 GHz bandwidth
- Moderate complexity modulation schemes

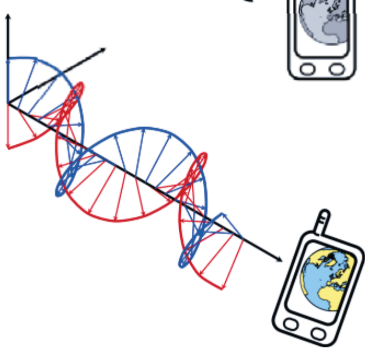
} ➔ 100 Gbit/s +

- CMOS PA technology readily available
- Equipment available at TUB and TUHH
- System implementation feasible in near future

Array-based Communiction Systems

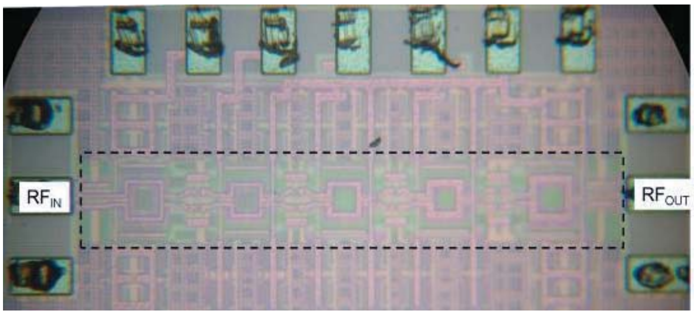
- Arrays for
  - Free space power combining
  - System scalability
  - Beam forming or beam steering
  - MIMO
- Circular polarization
  - Antenna alignment uncritical
- Dual polarization
  - Double data rate
  - Relaxed link budget requirements





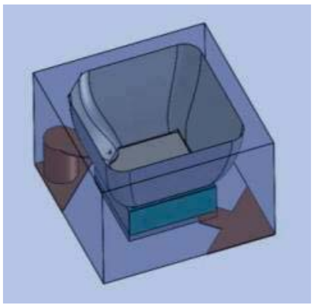
Low-cost Technologies

- CMOS technology
  - Highest integration density
  - Mixed signal SoC
  - High reliability
  - Cheap mass production



60 GHz CMOS PA with 0.27 mm^2 chip area

- Polymer process:
  - Vertical growth by polymer deposition and UV-curing
  - Inclined metalized walls
  - Fine resolution (µm scale)
  - Reliable interconnects



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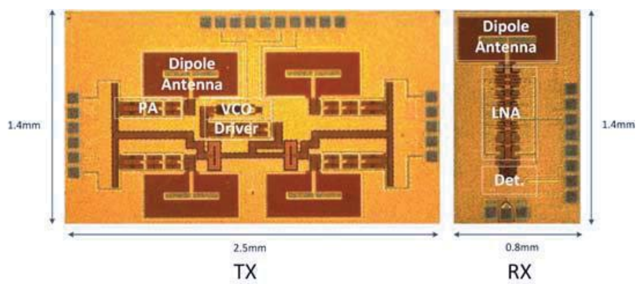
CMOS Power Amplifier

State of the Art

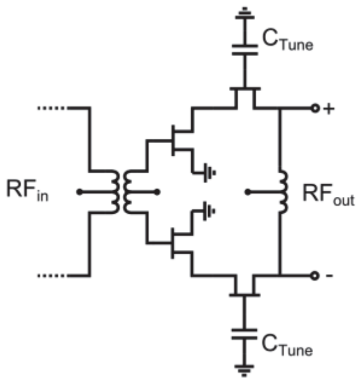
- Systems demonstrated up to W-band
- Circuits and components up to 300 GHz
- Low PAE with increasing BW
- → No high PAE broadband PA available



[1] Z. Wang et al. – ISSCC 2013, pp. 136 -137.

Concepts

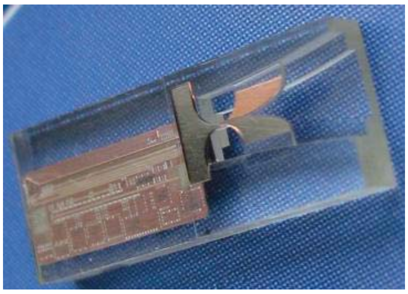
- Large signal cascode
- Differential design
  - Small source inductance
  - High gain
  - High output impedance
  - Low output loss/ high PAE
  - High bandwidth



Integrated Antenna Array

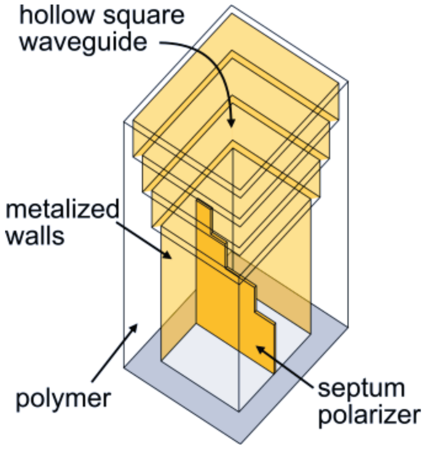
State of the art
- Antenna-on-chip
  - Poor performance
  - Limited functionality
  - Large area even above 100 GHz
  - Arrays costly to realize
- Antenna-in-package
  - Wideband system-in-package [2]
  - Up to W-band

➔No broadband circular polarized arrays



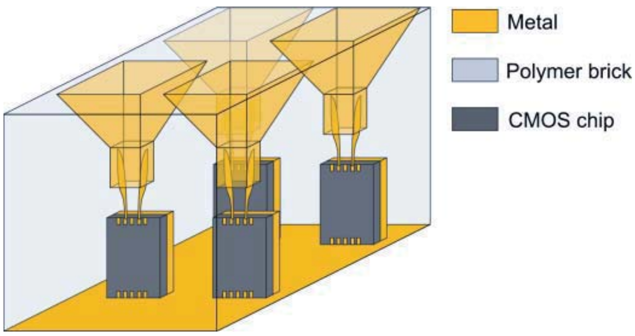
[2] L. Tripodi et. al – Trans. MTT, 60, No. 12.

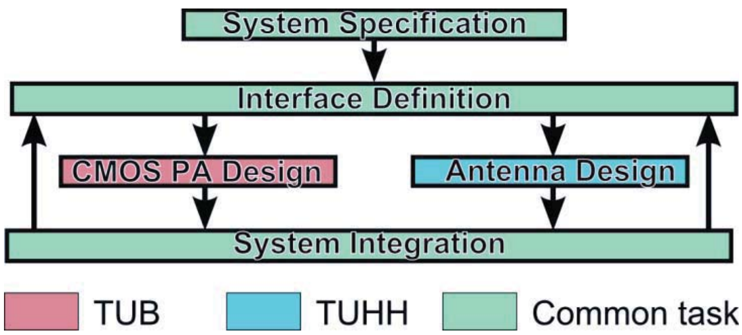
Concepts
- 3D integrated horn antenna
  - Polymer process
  - Dual circular polarization



System Integration Concepts

- Brick architecture
- PA-antenna interface
  - Geometry (e.g. pad layout)
  - Balanced feed
  - Matched to PA impedance
- Basic demonstrators





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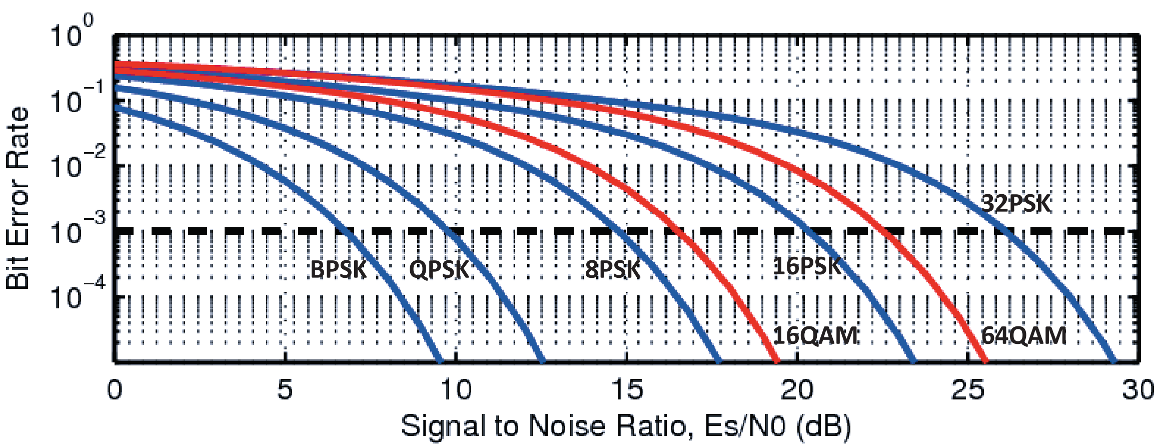
Modulation Schemes: SNR

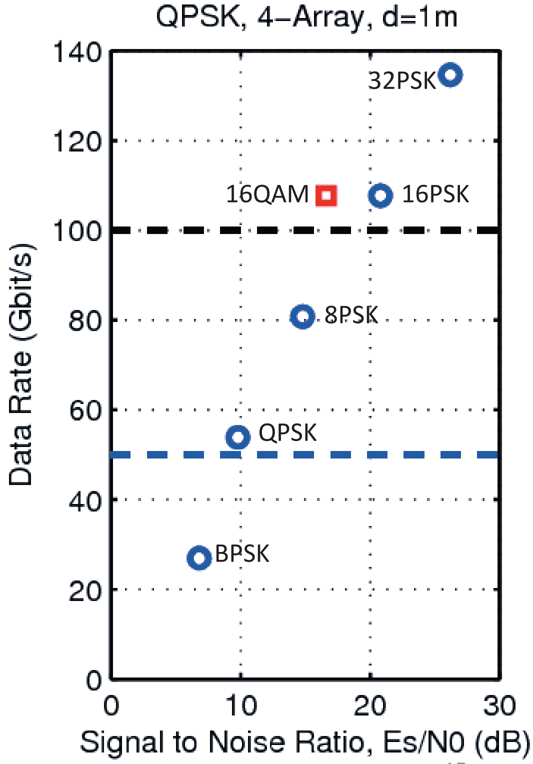
- Assume: - Forward Error Correction (FEC)
  - Pre-FEC Bit Error Rate (BER) ≤ 10^{-3}
  - AWGN channel
- SNR limit from BER plots:



- Example: SNR of 9.8 dB (QPSK) or 14.8 dB (8PSK) required.

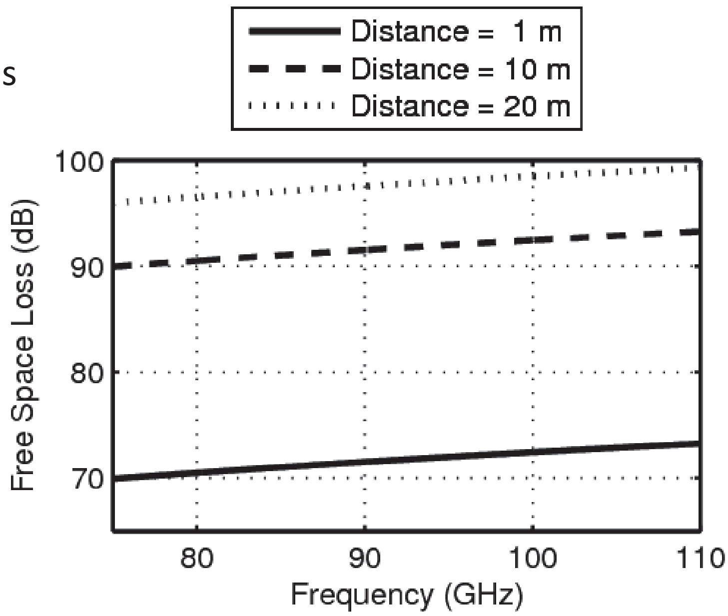
Modulation Schemes: Data Rate

- 50 Gbit/s per polarization (dashed line)
- Raised-cosine filter for pulse-shaping
  $B' = B/(1 + r)$, with r = 0.3.
  ➔ Data Rate = 27 Gbit/s · $\log_2 m$.
- FEC further reduces net data rate.
- **QPSK**: (54 GBit/s, SNR=9.8 dB)
  8PSK: (81 GBit/s, SNR=14.8 dB).
- Single polarization needs $m \geq 16$.



Scenarios: Free-Space Loss

- Free-space loss for different scenarios (worst case):
  - 1 m ➔ 73 dB
  - 10 m ➔ 93 dB
  - 20 m ➔ 99 dB
- Loss varies across band
- Additional losses for PA and LNA packaging (about 1.5 dB each).



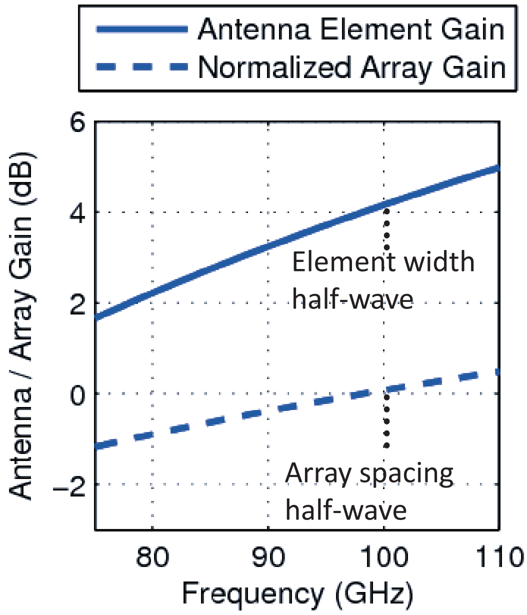
Tx: Power-combining and Array Gain

- CMOS PA at 5 dB backoff [3]
  P_{Tx} = 10 dBm

- Antenna gain of rect. waveguide:
  $G = 4\pi \cdot \eta_{rad} \cdot (A_{rect} / \lambda^2)$

- For +/- 45° max. scan angle element spacing d ≤ 0.56 λ
  ➔ d_{max} = 1.5 mm @ 110 GHz

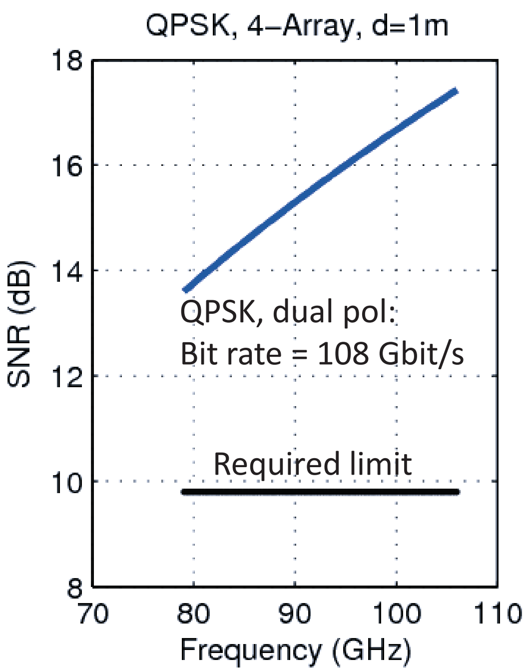
- ***N* elements** for Tx.
- **One element** for Rx (for now).



Number of Array Elements

- Friis transmission equation:
  - $P_{Rx} = N \cdot P_{Tx} \cdot N_{eff} \cdot G_{Tx} \cdot G_{Rx} / L$
- CMOS LNA: F = 8 dB, G=20 dB [4].
- $SNR = P_{Rx} / k_B T_0 BF$ after CMOS LNA
- **Goal**: Solve for number of elements N

Mod.	Required # of Tx-Array Elements 1m	10m	20m	Data Rate, dual pol.
BPSK	2	19	37	54 GBit/s
QPSK	3	26	52	108 GBit/s
8PSK	5	46	92	162 GBit/s



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Conclusions

- **Conclusions**
  - System development for
    - Operation at W-band
    - Dual circular polarization
    - Antenna array
    - Low-cost technologies (CMOS, 3D polymer process)
    - Scalable approach
  - Integration concept for PA + antenna
    - Interfaces between PA/Ant (geometry, impedance)
  - System budget analysis shows:
    - Short range (1m) with 2x2 Tx-array
    - Medium range (10m, 20m) with 5x6 or 7x8 Tx-array

Thank you for your attention

References

- [1] Z. Wang et al.: „*A 210GHz fully integrated differential transceiver with fundamental-frequency VCO in 32nm SOI CMOS*," ISSCC 2013, pp. 136 -137, San Francisco, Feb. 2013.
- [2] L. Tripodi et. al.: „*Broadband CMOS Millimeter-Wave Frequency Multiplier With Vivaldi Antenna in 3-D Chip-Scale Packaging*," IEEE Trans. MTT, Vol. 60, No. 12, pp. 3761–3768.
- [3] K.-J. Tsai et. al.: "*A W-band Power Amplifier in 65-nm CMOS with 27GHz Bandwidth and 14.8dBm Saturated Output Power*," RFIC 2012, pp. 69 – 72, Montreal, June 2012.
- [4] D.-R. Lu et. al.: "*A 75.5-to-120.5-GHz, high-gain CMOS low-noise amplifier*" – IMS 2012, Montreal, June 2012.