A New View on Analogue-Digital-Balance with System Design

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Making Bits Fly

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   – Phase modulated clock
   – Recursive Filter
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1. What's going on? - Challenges of the future

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What's going on? - Challenges of the future
Moore‘s law

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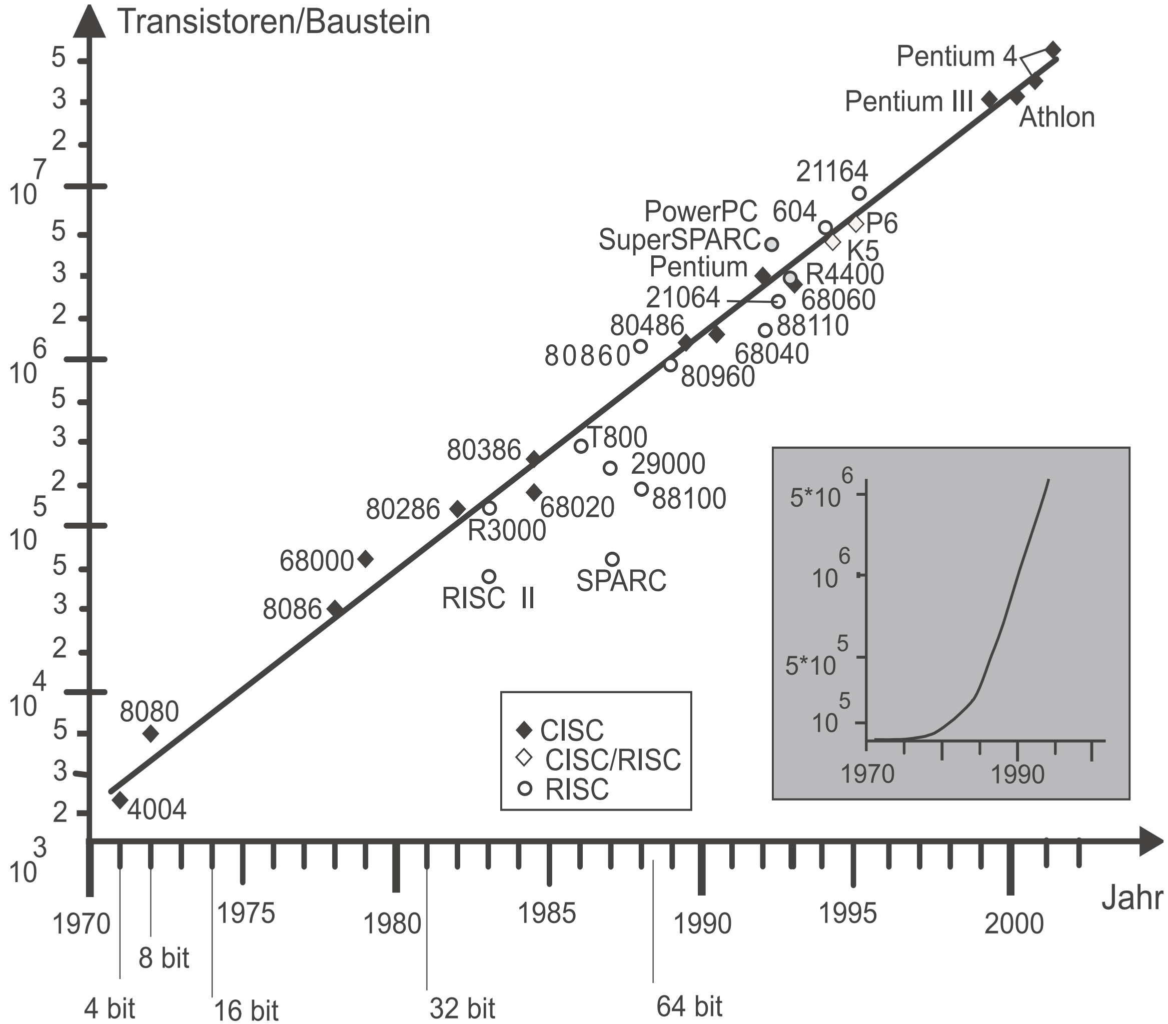
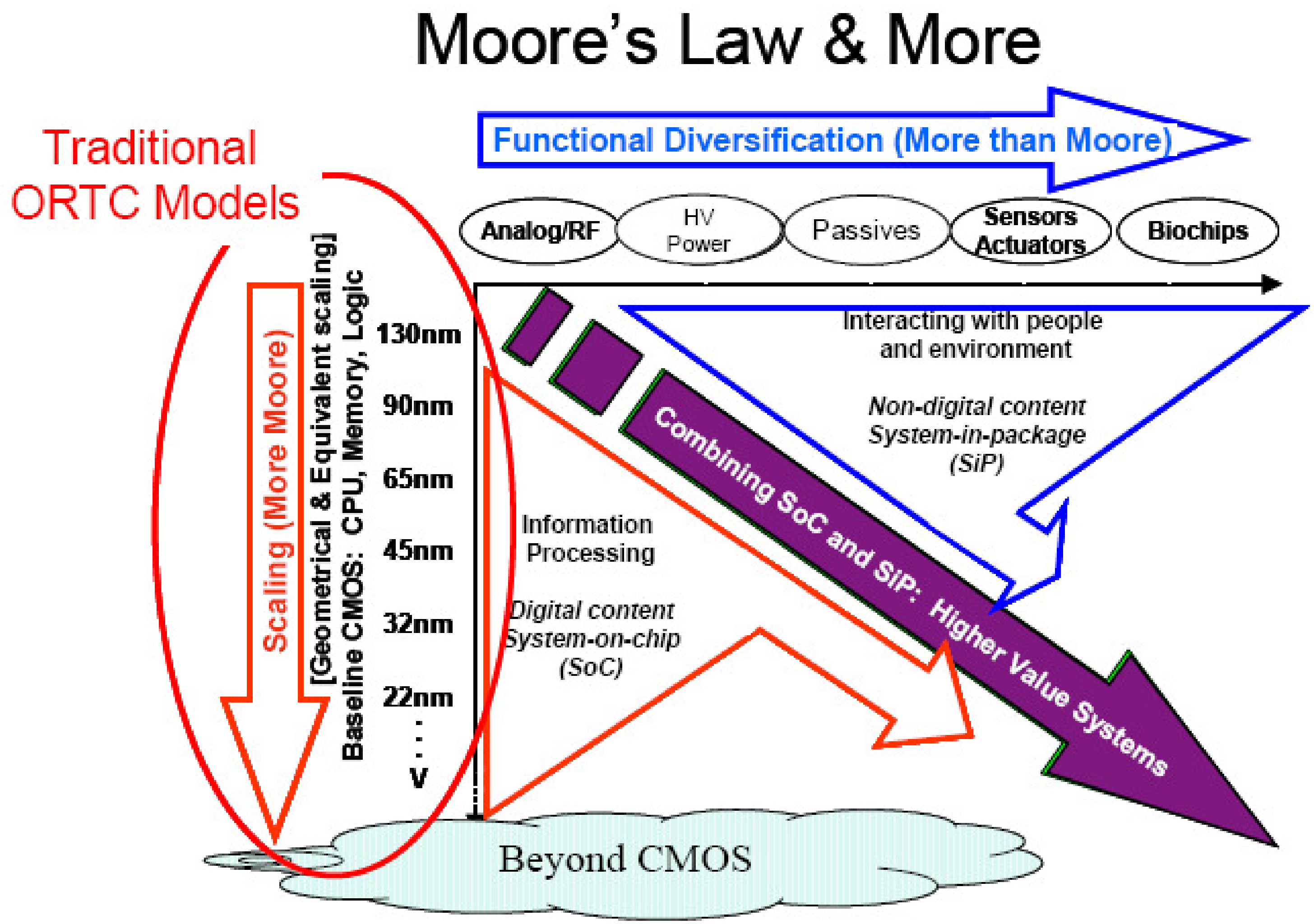
Gordan Moore, TI 1965:
"Complexity of an IC is doubling every 2 years"



Quelle: H. Bähring, *Mikrorechnertechnik,* Band , Springer, 2002.

➔ Integration density of Electronics is doubling every two years

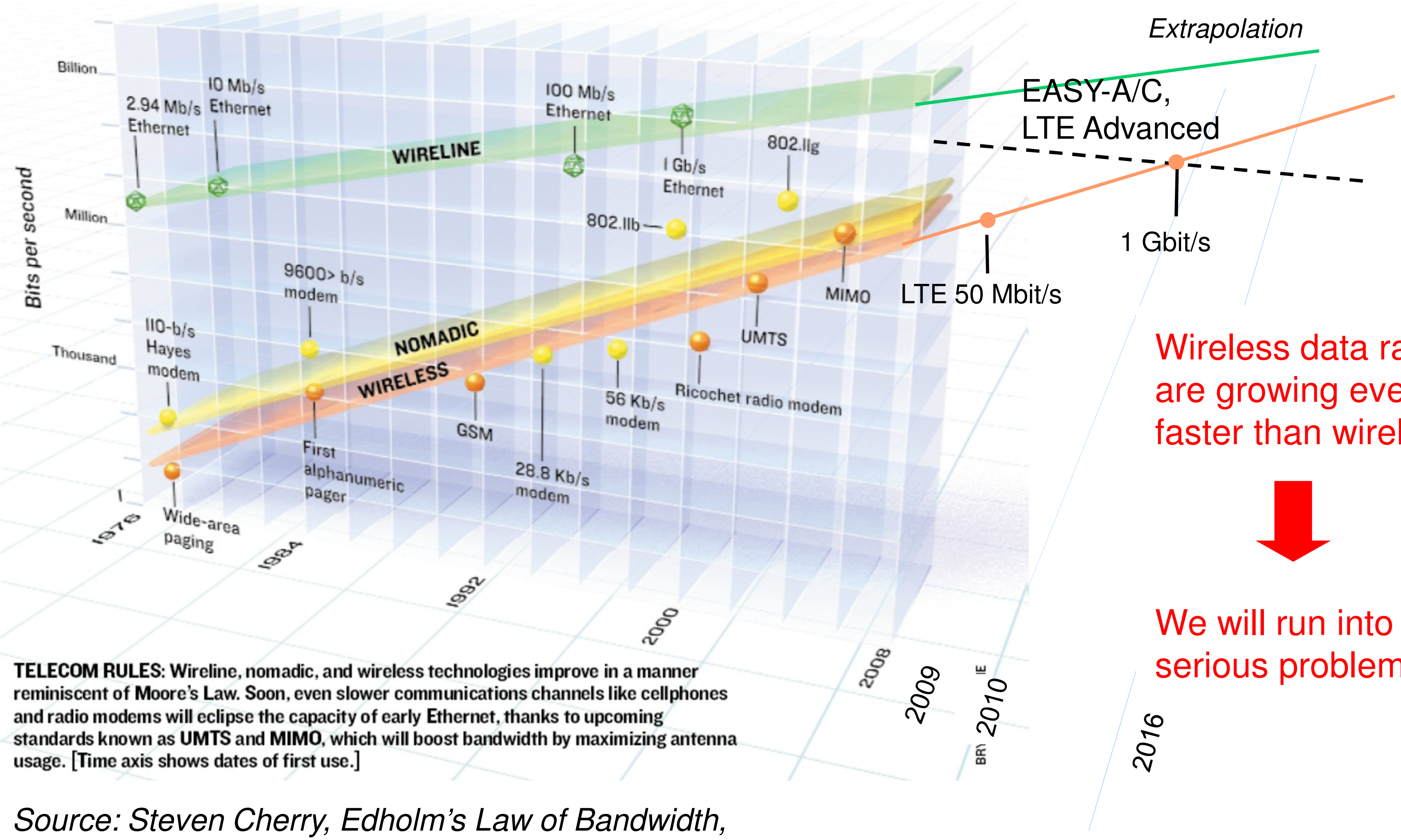
What’s going on? - Challenges of the future
ITRS Roadmap



Source: INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (ITRS) 2009 EDITION

What's going on? - Challenges of the future

Edholm's law of bandwidth



Wireless data rates are growing even faster than wireline!

We will run into a serious problem!

Source: Steven Cherry, Edholm's Law of Bandwidth,
Telecommunications data rates are as predictable as Moore's Law, IEEE Spectrum, July 2004
Phil Edholm, Nortel's chief technology officer and vice president of network architecture

What's going on? - Challenges of the future
Analysis by APWPT

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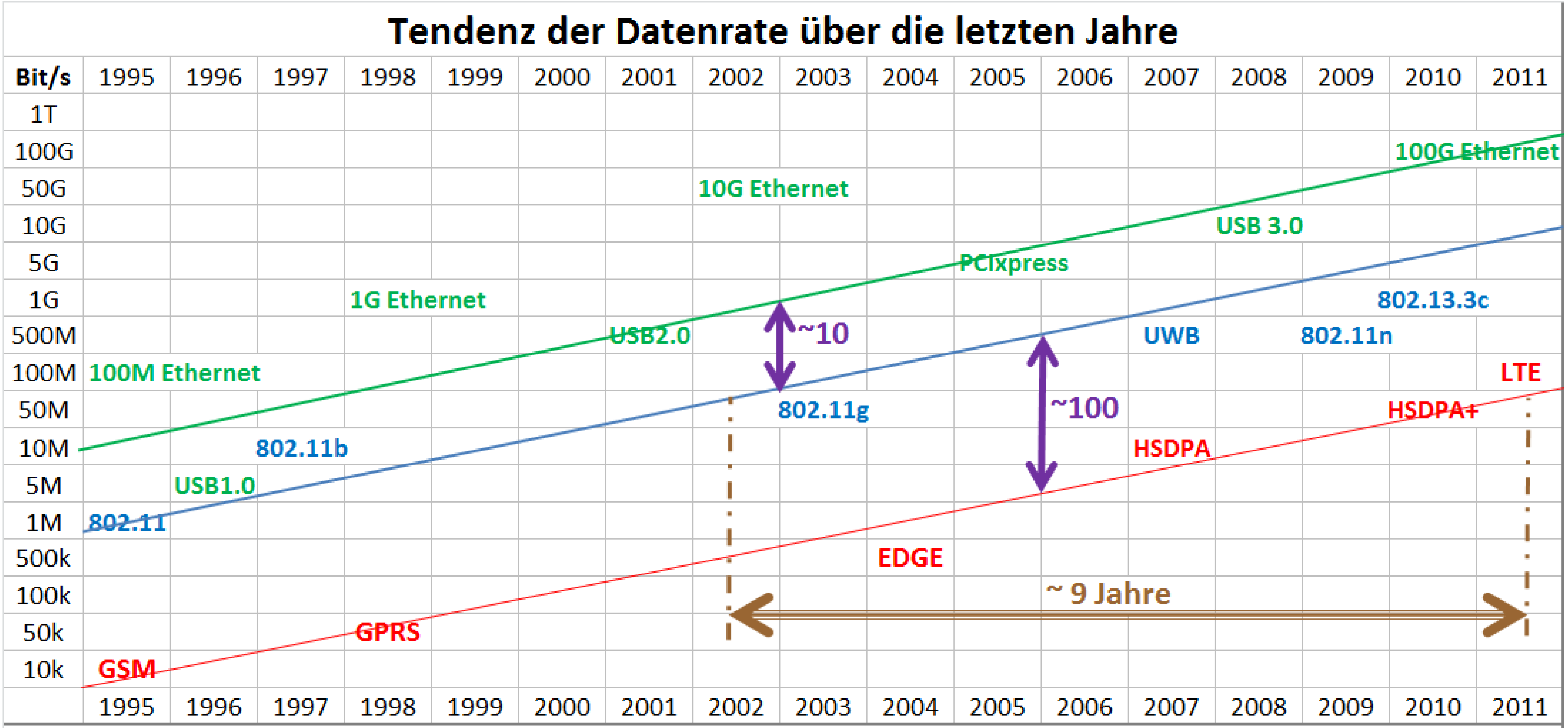


Legende:

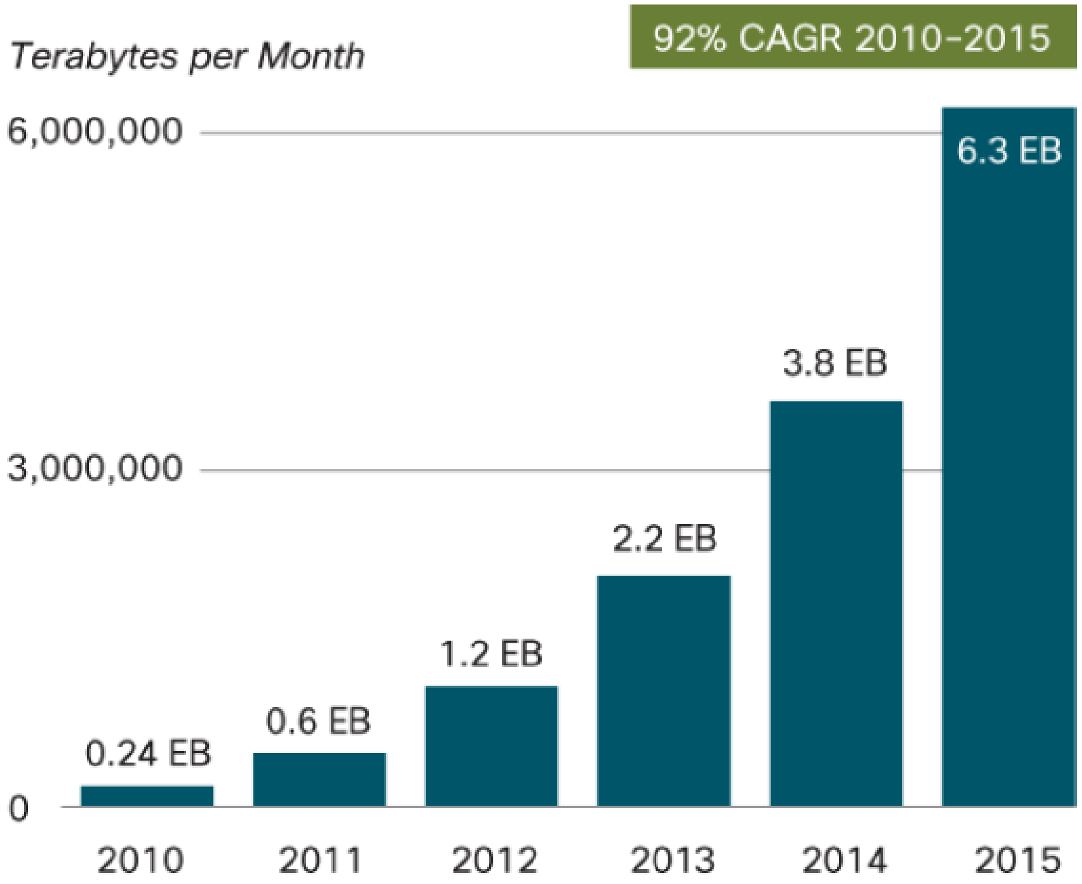
Source: M. Fehr, APWPT

Kabelverbindung
WLAN
Mobilfunk

➔ Data Rate is doubling every two years

What's going on? - Challenges of the future
CISCO study

Figure 1. Cisco Forecasts 6.3 Exabytes per Month of Mobile Data Traffic by 2015

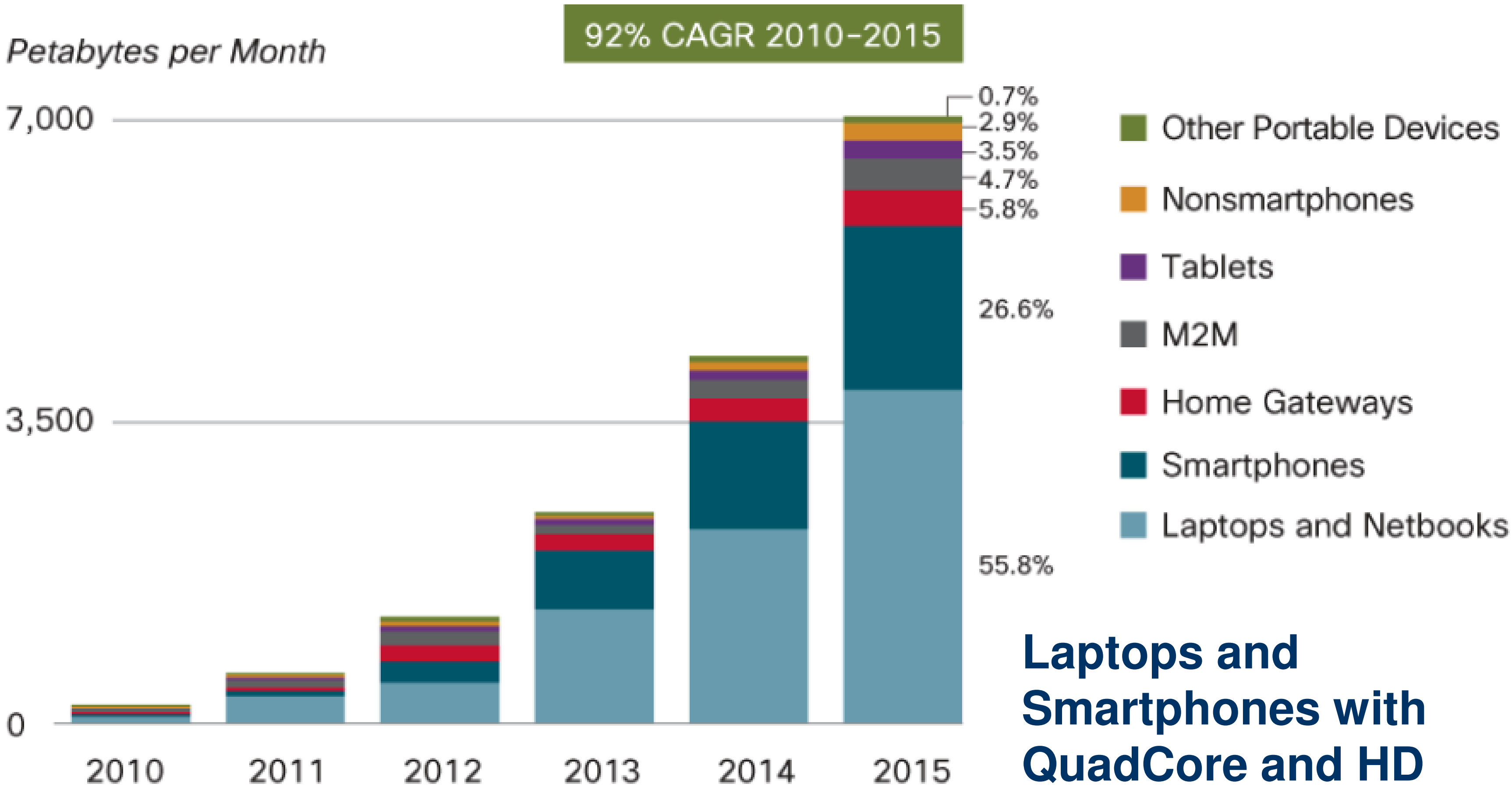


Source: Cisco VNI Mobile, 2011

➔ Mobile Communication Data amount is Doubling each year!

What's going on? - Challenges of the future
CISCO study

Figure 3. Laptops and Smartphones Lead Traffic Growth

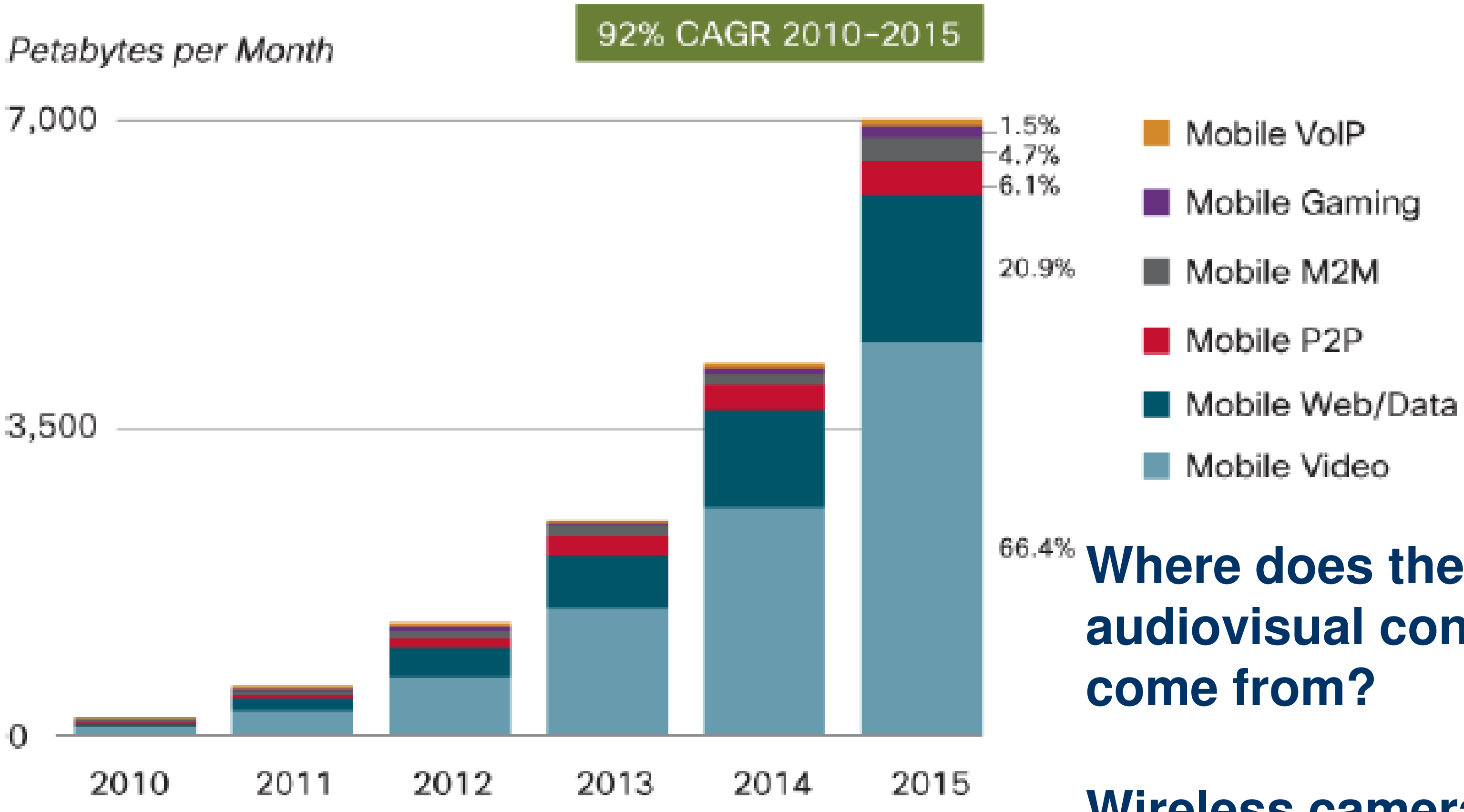


Source: Cisco VNI Mobile, 2011

Laptops and Smartphones with QuadCore and HD Display…

What’s going on? - Challenges of the future
CISCO study

Figure 5. Mobile Video Will Generate 66 Percent of Mobile Data Traffic by 2015



VoIP traffic forecasted to be 0.4% of all mobile data traffic in 2015.

Source: Cisco VNI Mobile, 2011

Where does the audiovisual content come from?

Wireless cameras, wireless microphones, so PMSE…

What's going on? - Challenges of the future
Immersive perception

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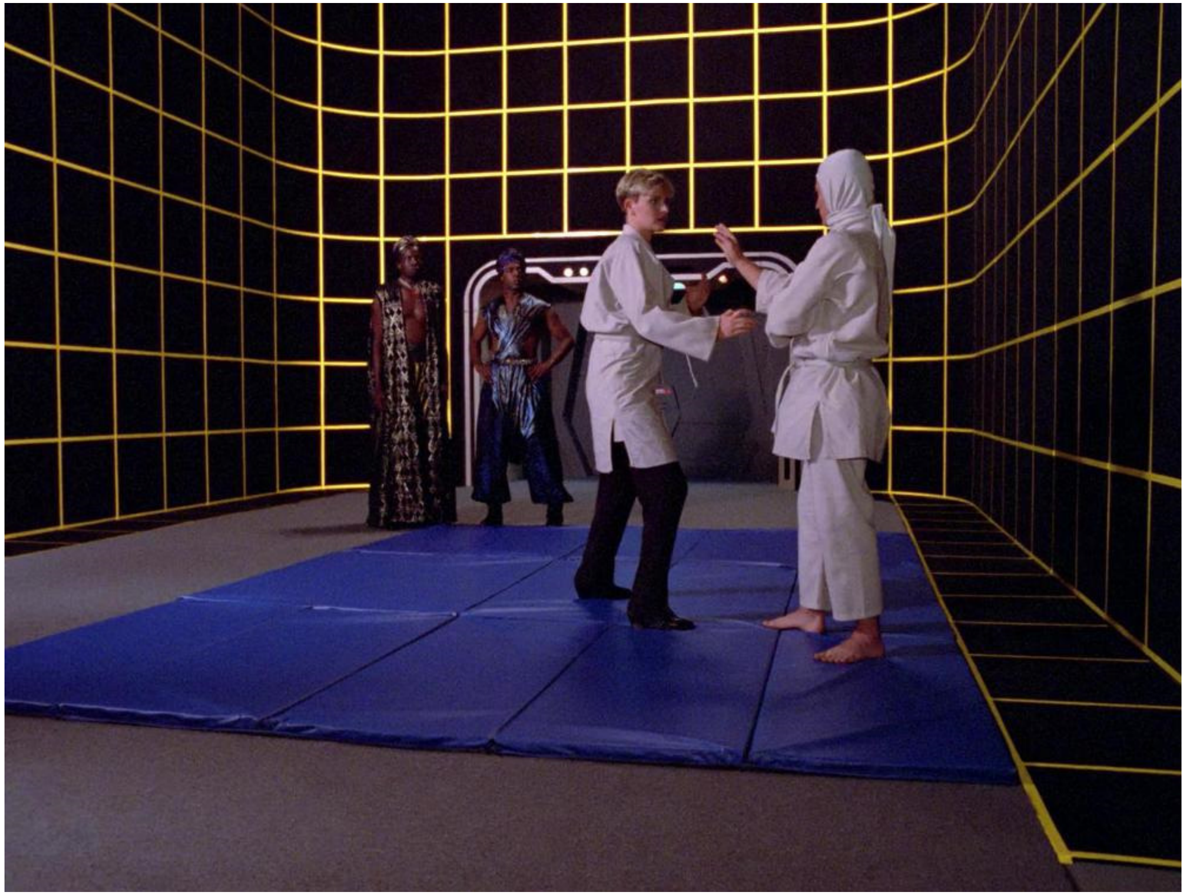


Holodeck, telepresence

Source: Star Trek

Can we fully capture an event, performance?

Produce it ?

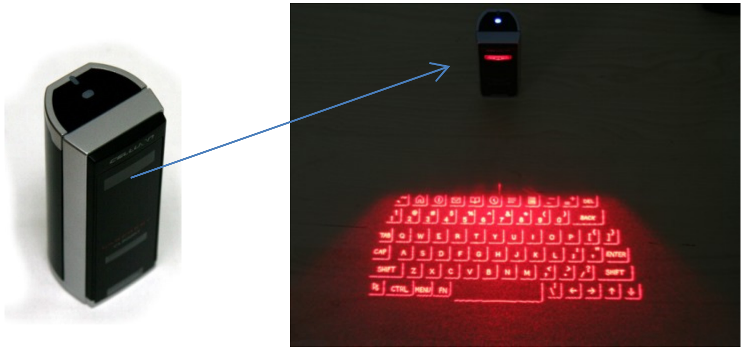
Reproduce it in an immersive way?

We are on the way by audio & video in HD, 3D, multichannel,…

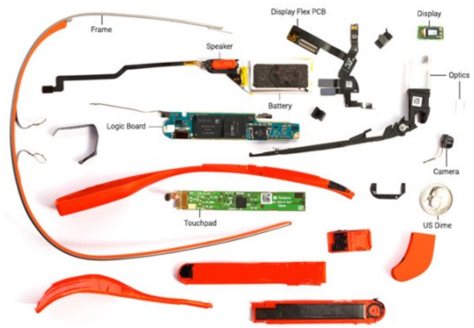
What's going on? - Challenges of the future
New Mobile MMIs

Google Glasses

Source: Microvision



Source: Celluon



Source EDN

Source: Microvision

Quadcore Smartphone LG

2. Evolution of Converter Technology

Evolution of Converter Technology

Walden paper (Analog Devices) – ADC Snapshot 1999

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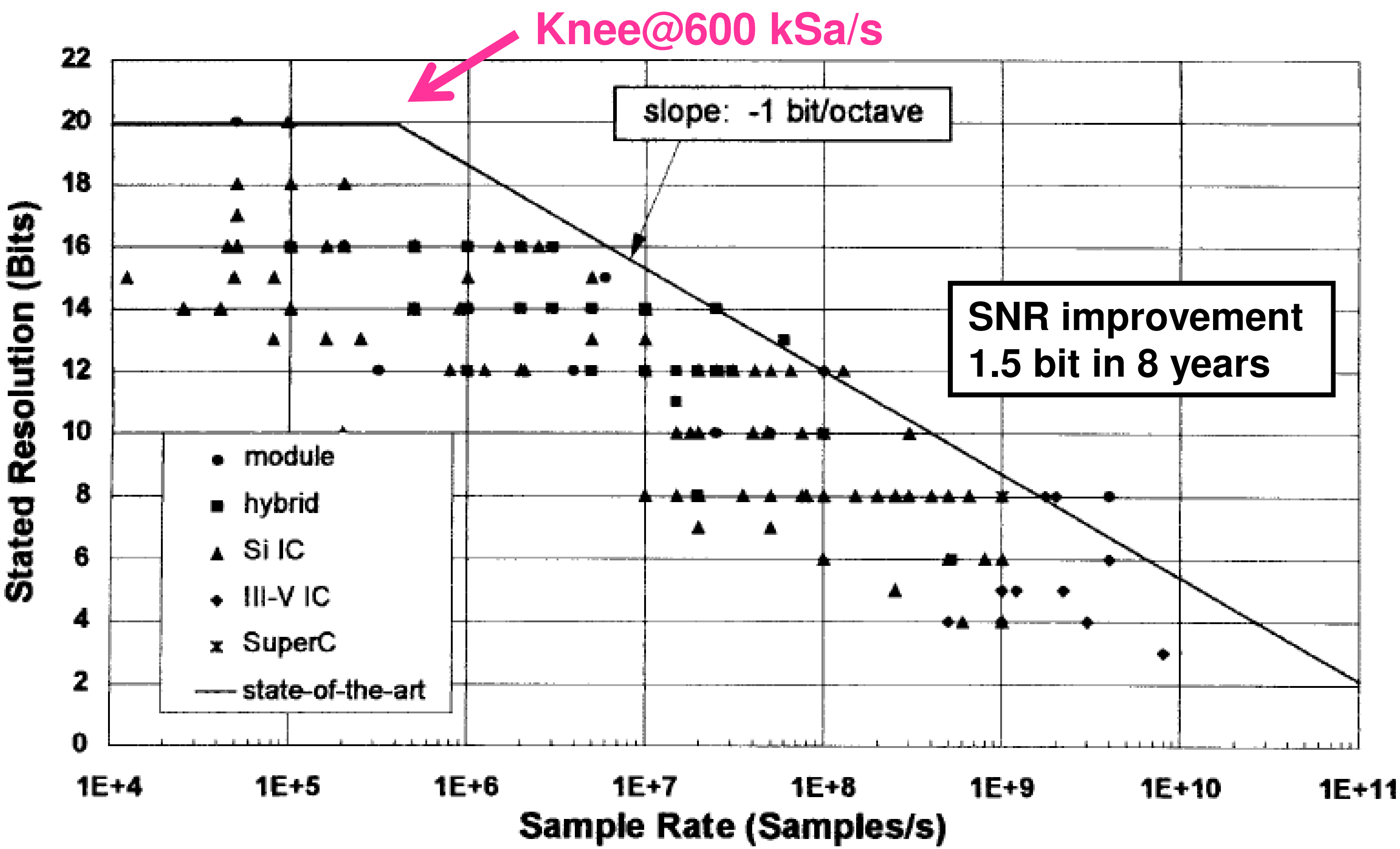
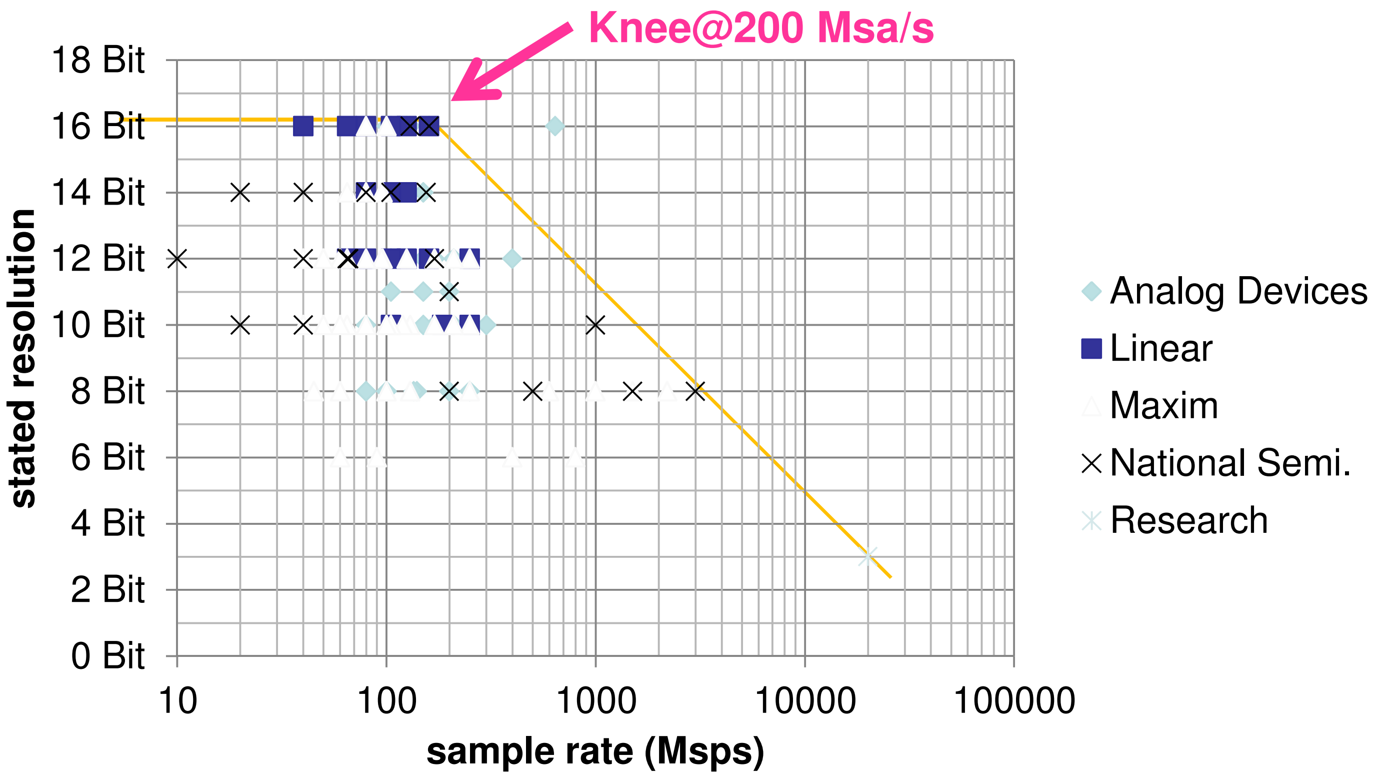


Source: Walden R.H., Analog-to-Digital Converter Survey and Analysis, IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS, VOL. 17, NO. 4, APRIL 1999, p539

Evolution of Converter Technology

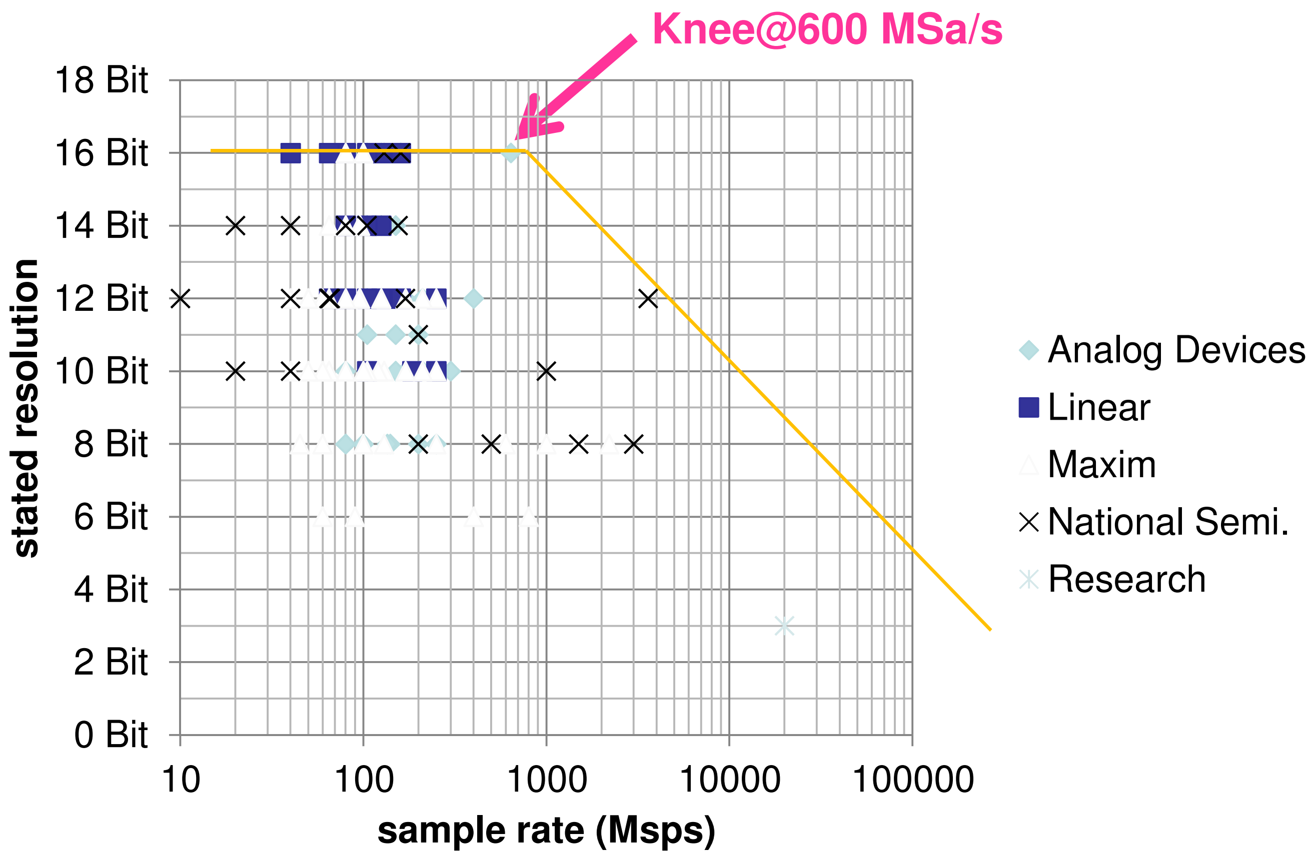
ADC Snapshot 2009



Findings

- The rule "*1 bit is lost for doubling frequency*" still holds,
  6 dB SNR is lost, but only 3 dB process gain is gained – so it doesn't pay off
- The knee shifts with technology evolution
- 200 MSa/s the only reasonable sampling rate for SDR - today
- Limits us to roughly 50 MHz air interface for highest dynamic range!

Evolution of Converter Technology
ADC Snapshot 2010



Findings

- High Momentum in shifting the knee
- Moore's law is working for the knee shift

Most Recent figures

- ADC: 3.6 GSa/s @12 bit and DAC: 2.4 GSa/s @16bit

Evolution of Converter Technology
DAC Snapshot 2010

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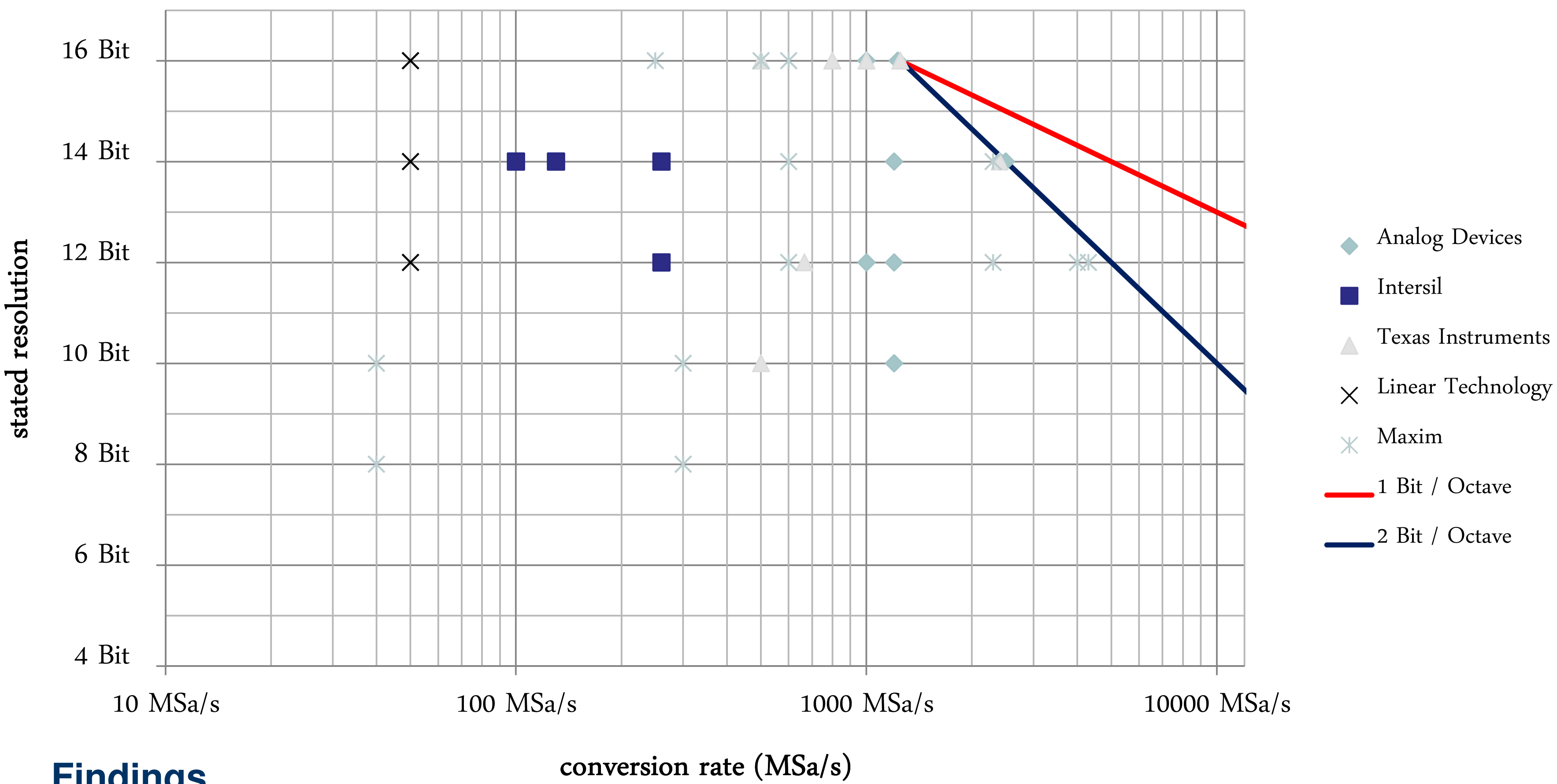

Findings

- DAC far ahead of ADC
- 2 bit/octave limit
- Moore’s law is also working for the knee shift

Evolution of Converter Technology
Walden Knee

3. Systematic partioning into A/D

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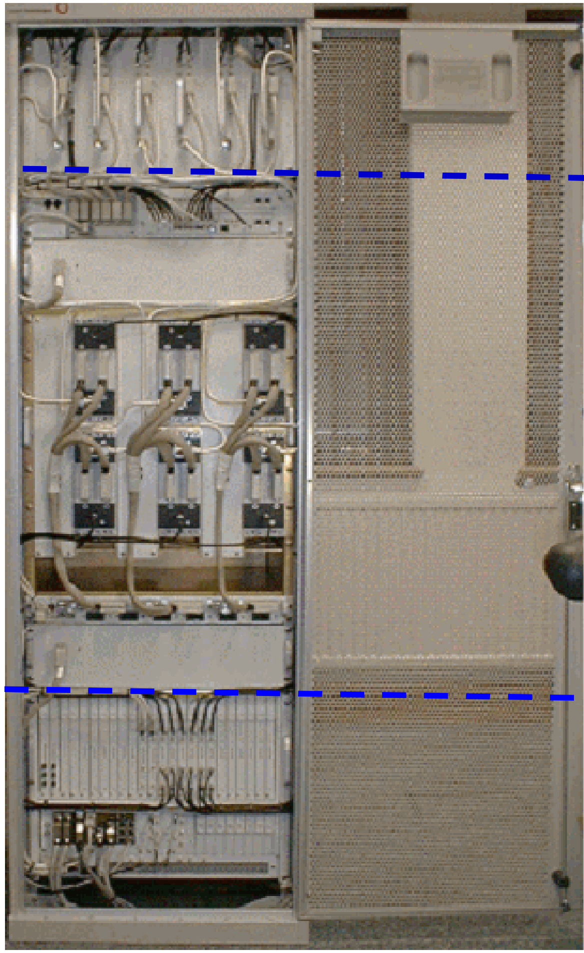
Systematic partioning into A/D
Basestation cabinet

Analogue
- 75% form factor
- Doesn't follow Moore's law
- Innovation at architectural level necessary

Digital
- 25% form factor
- Follows Moore's law
- 20 nm CMOS helps...



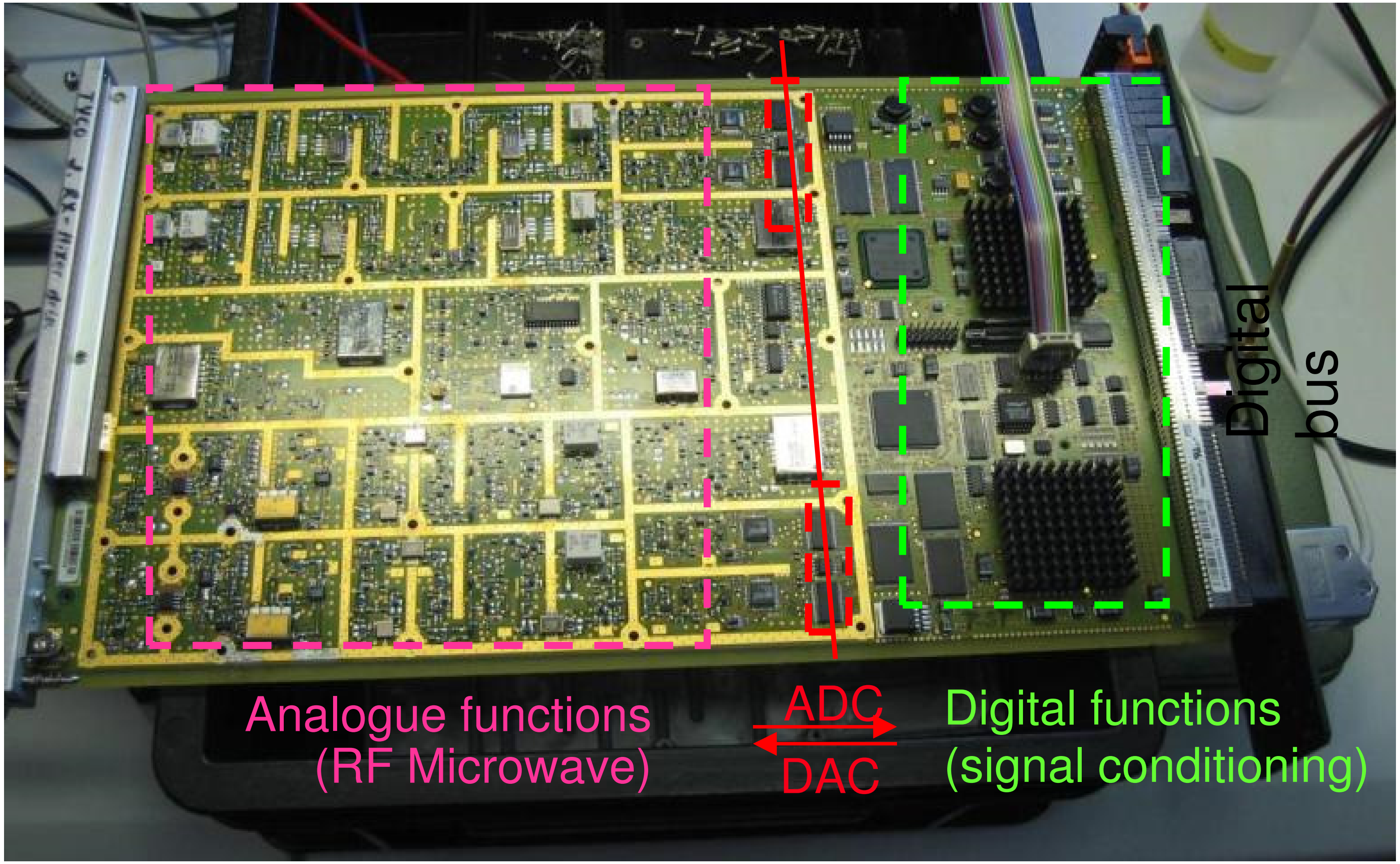
Source: Alcatel-Lucent OneBTS

25% form factor
Coaxial resonators
(12 filter für 3 sector 4 branch MIMO)

50% form factor
PA and cooling
(12 PAs für 3 sector 4 branch MIMO)

Systematic partioning into A/D

Basestation radio card



Source: Alcatel-Lucent OneBTS radio card

Systematic partioning into A/D

Pros and Cons

	Analogue	Digital
Aging	strong	no
Temperarture Drift	strong	no
Predictable performance	partly	yes
Scales with Moore's law (price erosion)	partly	yes
reconfiguration	possible	easy
Filters (Performance in light of realization effort)	moderate	Very High
Immunity to EMC	moderate	high
Capacity bit/s (Shannon equivalent)	high	moderate

Findings

- The arguments pro digital are very strong, but…
- Analogue is very beneficial in terms of capacity
  - Digital: 200 MSa/s@16bit=3.2Gbit/s
  - Analogue: 500 MHz@100 dB SNR=16.6 Gbit/s

$$C = BW \cdot ld\left(1 + \frac{S}{N}\right)$$

Systematic partioning into A/D
4 Quadrants

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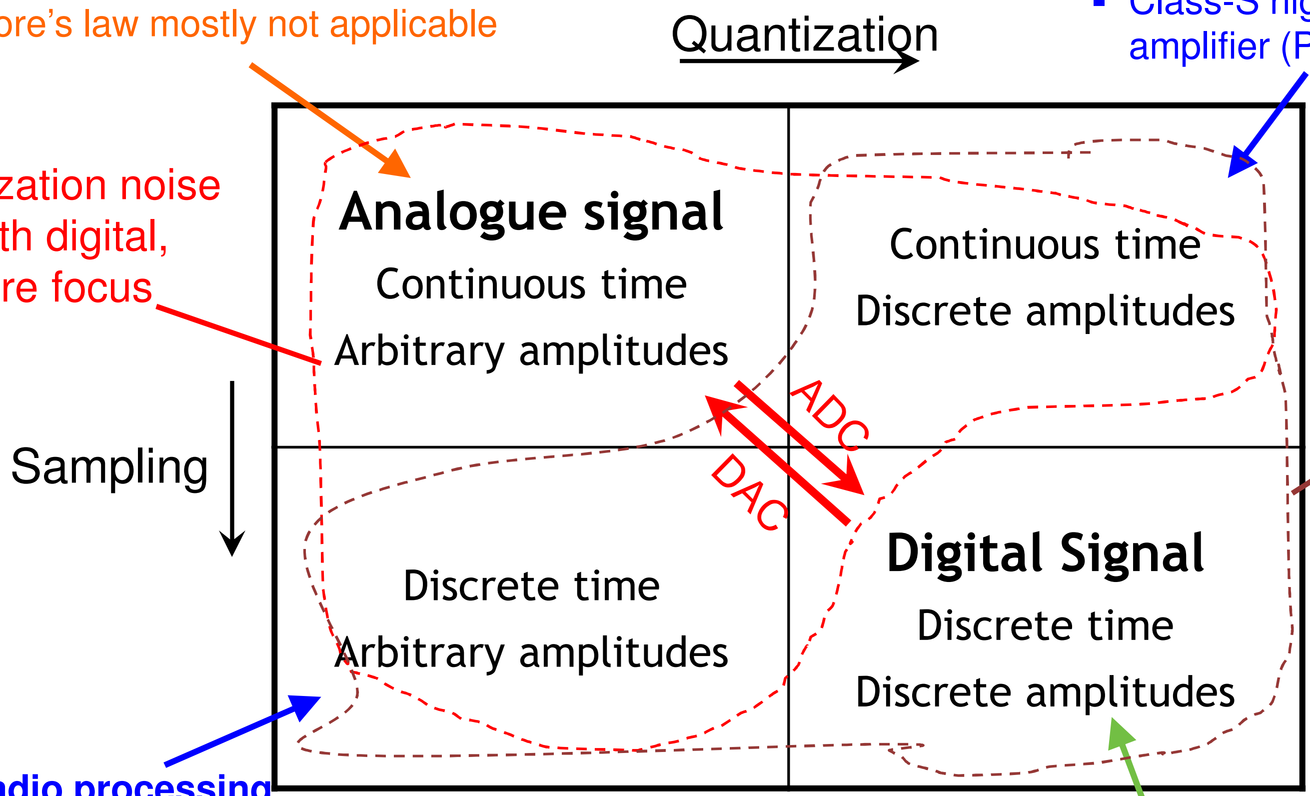
Domain of classical RF/Microwave
- e.g. Class-AB power amplifier
- Moore's law mostly not applicable

Digital Radio Processing
- Switch mode PA Class-D/E/F
- Class-S high speed digital amplifier (PWM)

Quantization noise only with digital, therefore focus here



Profit from Moore's law by architecture innovation

Digital radio processing
- Switched cap filter
- Digital PLL
- DCO Digital controlled Oscillator
- DCF Digital controlled filter

Domain of classical digital signal processing
- FPGA / ASIC / DSP
- Follows Moore's law
- Class-S with DSM

Systematic partioning into A/D

4 Quadrants

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Analogue
+ Capacity
- Aging/Drift
- Doesn't scale well
- Phase noise critical

PLM
+ Capacity
+ Scales well
+ Switch mode, high efficiency
- Short pulses, large f_T needed

Analogue signal Continuous time Arbitrary amplitudes	Continuous time Discrete amplitudes
Discrete time Arbitrary amplitudes	**Digital Signal** Discrete time Discrete amplitudes

Matches
CMOS, GaN, InGaP

Switched Cap
+ Capacity
+ scales well
- Jitter critical

Digital
+ Scales well
- Quantization noise
- Low capacity

Systematic partioning into A/D
How to move between Quadrants

Problem
- How to move from Digital Time discrete to time continuous?
- Massive Oversampling?
- 2 GSa/s to 200 GSa/s
- Only provides factor 100, so 20 dB process gain, equal to 3 bit

Solution
- Use a phase modulated clock
- Transition from time discrete -> time continuous

Issue
- Phase modulation of clock equal to PM
- We need conversion from IQ to polar
- Bandwidth enlargement by factor 5…7

Systematic partioning into A/D
Complexity assessment

Goal: One universal metric for analogue and digital

- Def.: Overhead factor
  - Amount of data relative to net data stream
  - Defined for each signal processing stage
- Net Data stream: Typical 12.2 kbit/s for voice
- Calculations:
  - Analog domain: Use Shannon
    B=bandwidth, SNR=Signal-to-Noise-ratio

    $$C_{Analog} = B \cdot ld\left(1 + \frac{S}{N}\right) = B \cdot ld\left(1 + 10^{SNR_{dB}/10}\right)$$

  - Digital domain:
    N=resolution, r=clock frequency

    $$C_{Digital} = N \cdot r$$

- Overhead factor:
  - By definition

    $$O_i = \frac{C_i}{12.2\,kbit/s}$$

  - Decoders output / Coders input:

    $$O_i = 1$$

  - air interface:

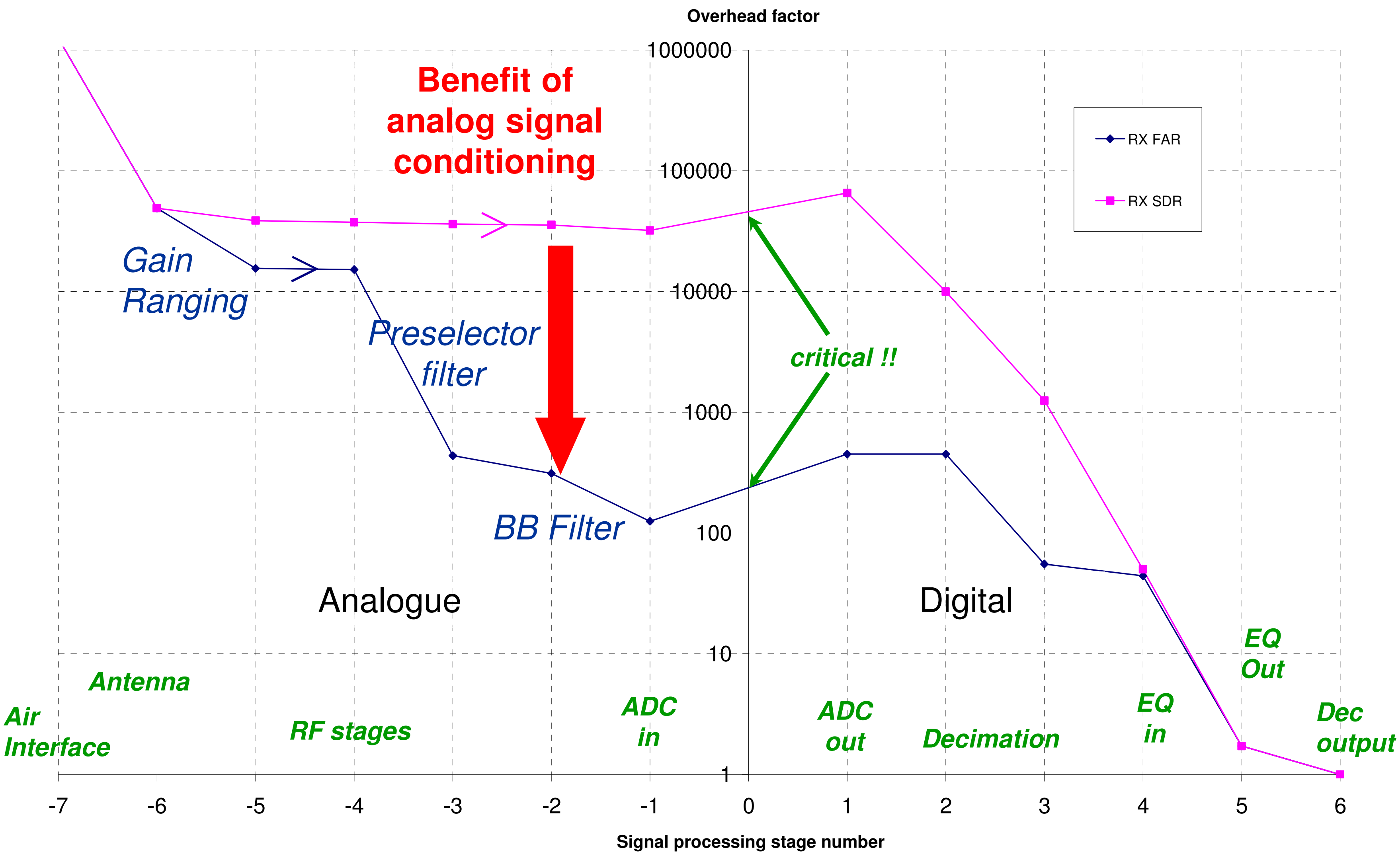
    $$O_i = \infty$$

- Method applicable for TX and RX

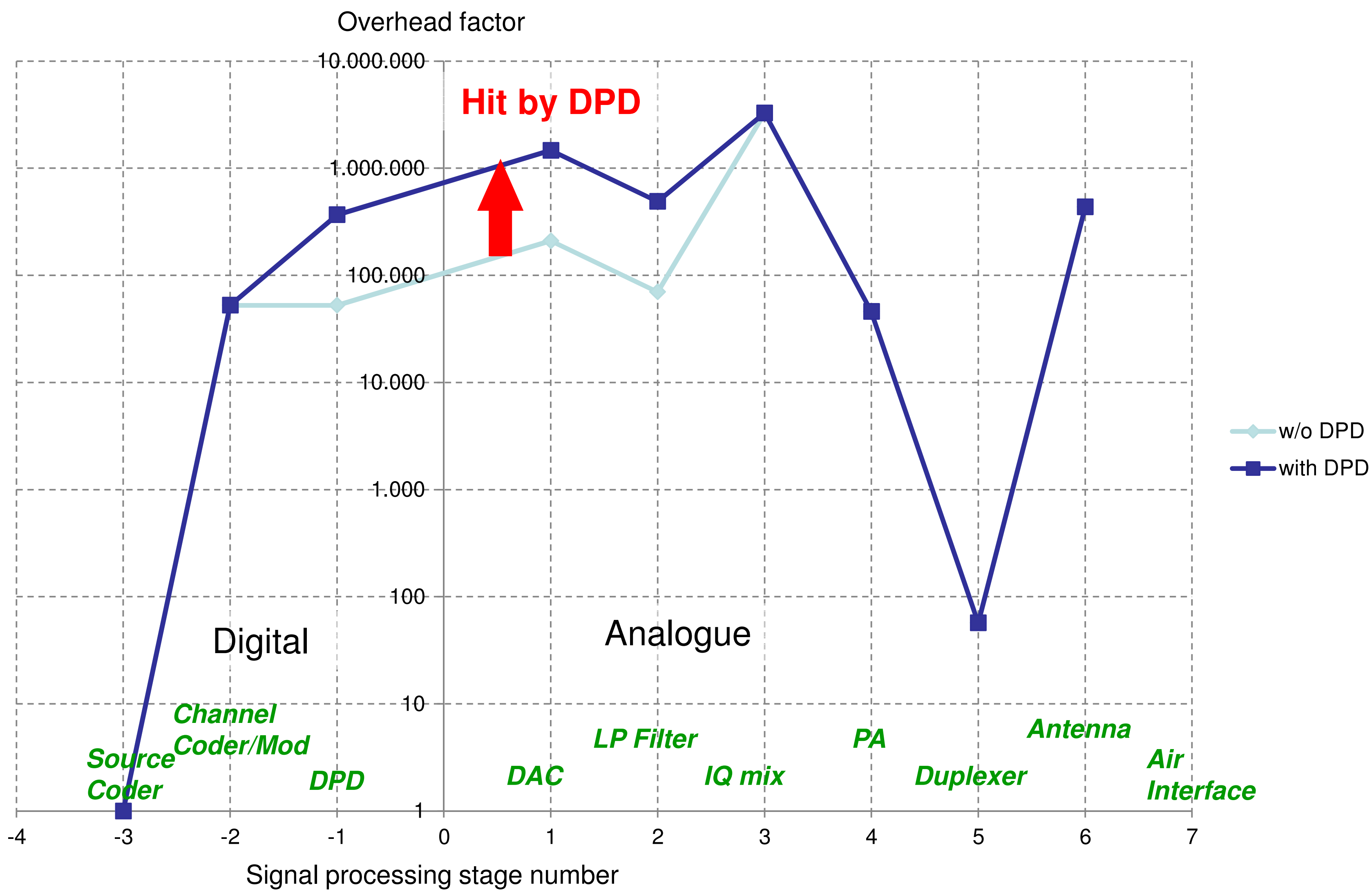
Patent: EP 1 521 738 B1, Method of analysing a receiver and/or transmitter chain, Filing date 4th October 2003, Proprietor: Lucent, Inventor: G. Fischer

Systematic partioning into A/D

Receiver Analysis for GSM



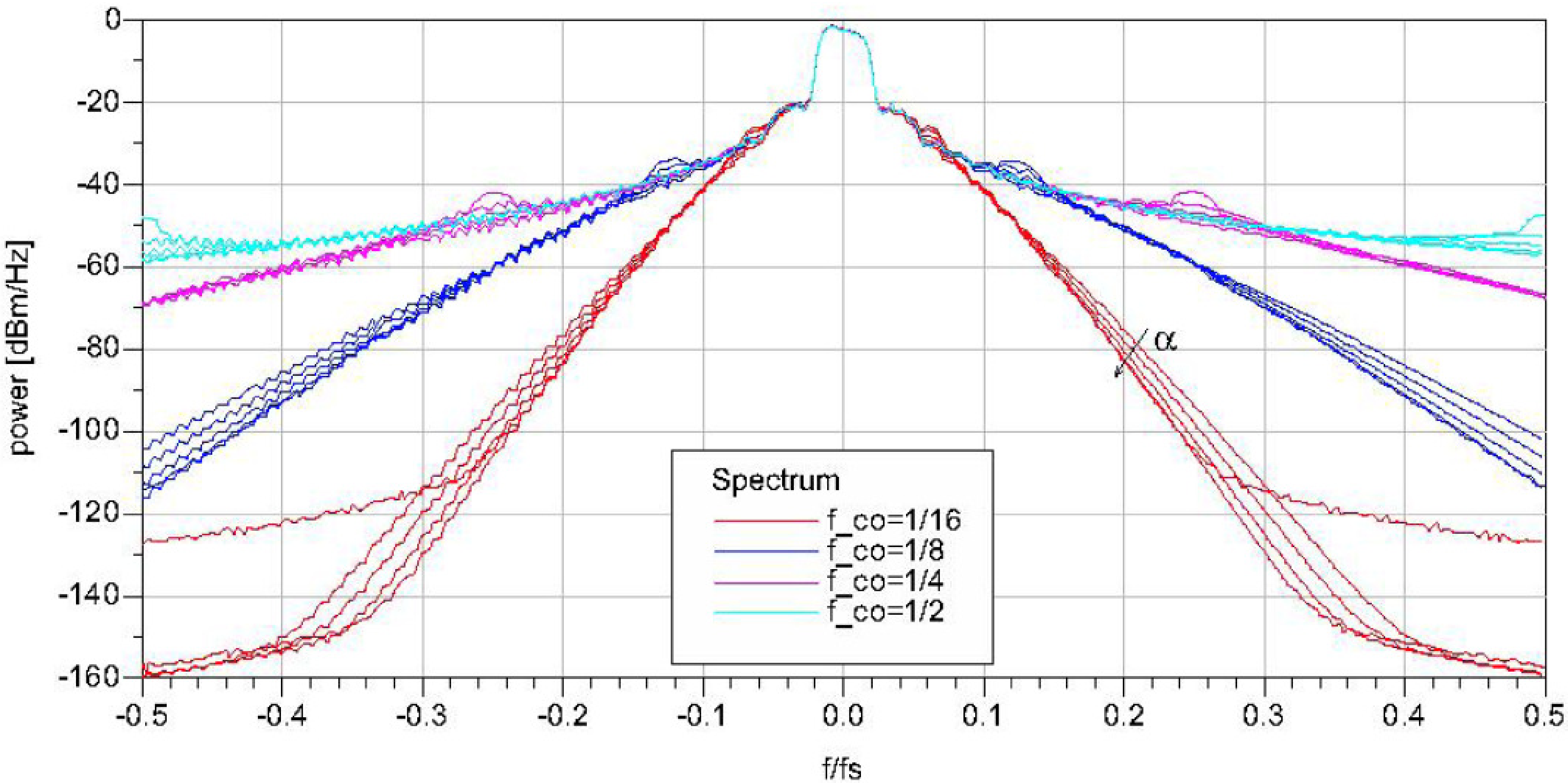
Systematic partioning into A/D
Transmitter analysis for LTE



4. Conversion from cartesian to polar

Conversion from cartesian to polar

Bandwidth Enlargement



Source: G. Strasser B. Lindner, L. Maurer, G. Hueber, A. Springer, On the Spectral regrowth in polar Tramsmitters, IEEE IMS 2006

➔ Cartesian to polar conversion increases bandwidth by factor 5...7 !

Conversion from cartesian to polar
Evolution of wideband air interfaces

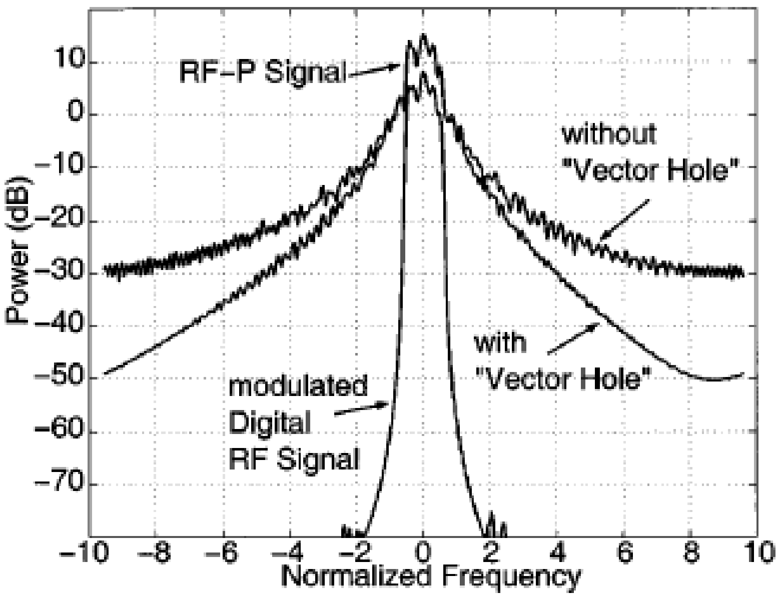


Fig. 5. Spectra of the RF-P and the modulated digital RF signal.

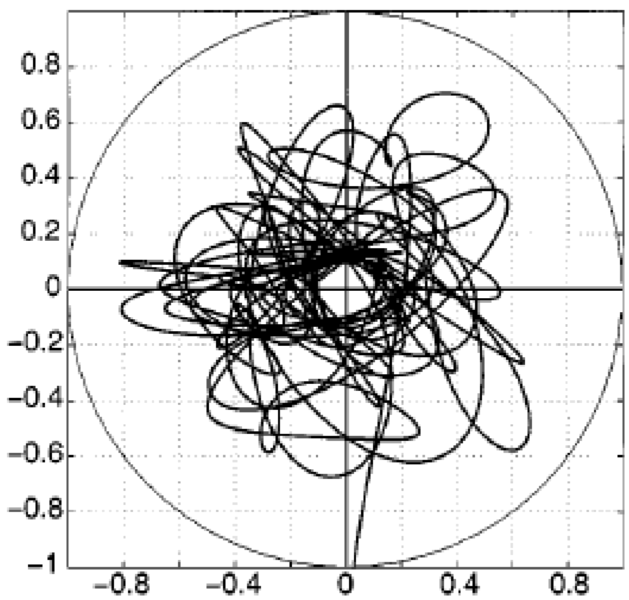


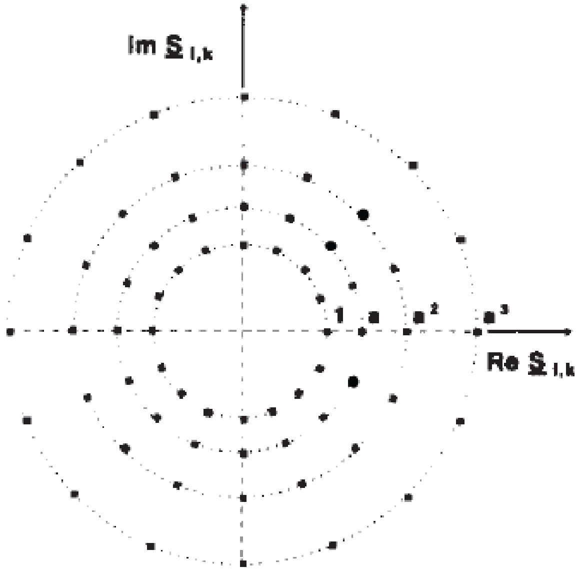
Fig. 6. Example of vector diagram of complex noise with a "hole."

Source: D. Rudolph, Out-of-Band Emissions of Digital Transmissions Using Kahn EER Technique, IEEE TRANS MTT, VOL. 50, NO. 8, AUGUST 2002

→ Zero crossing widens spectrum of phase even more

Minimize PAR (Peak to average ratio) and PMR (Peal to minimum ratio) by Clipping algorithms

Conversion from cartesian to polar
Modulation adapted to polar transmitters



64 DAPSK Characteristics

- 4 amplitude rings, log steps
- 16 phase states per ring
- Differential coding of amplitude and phase

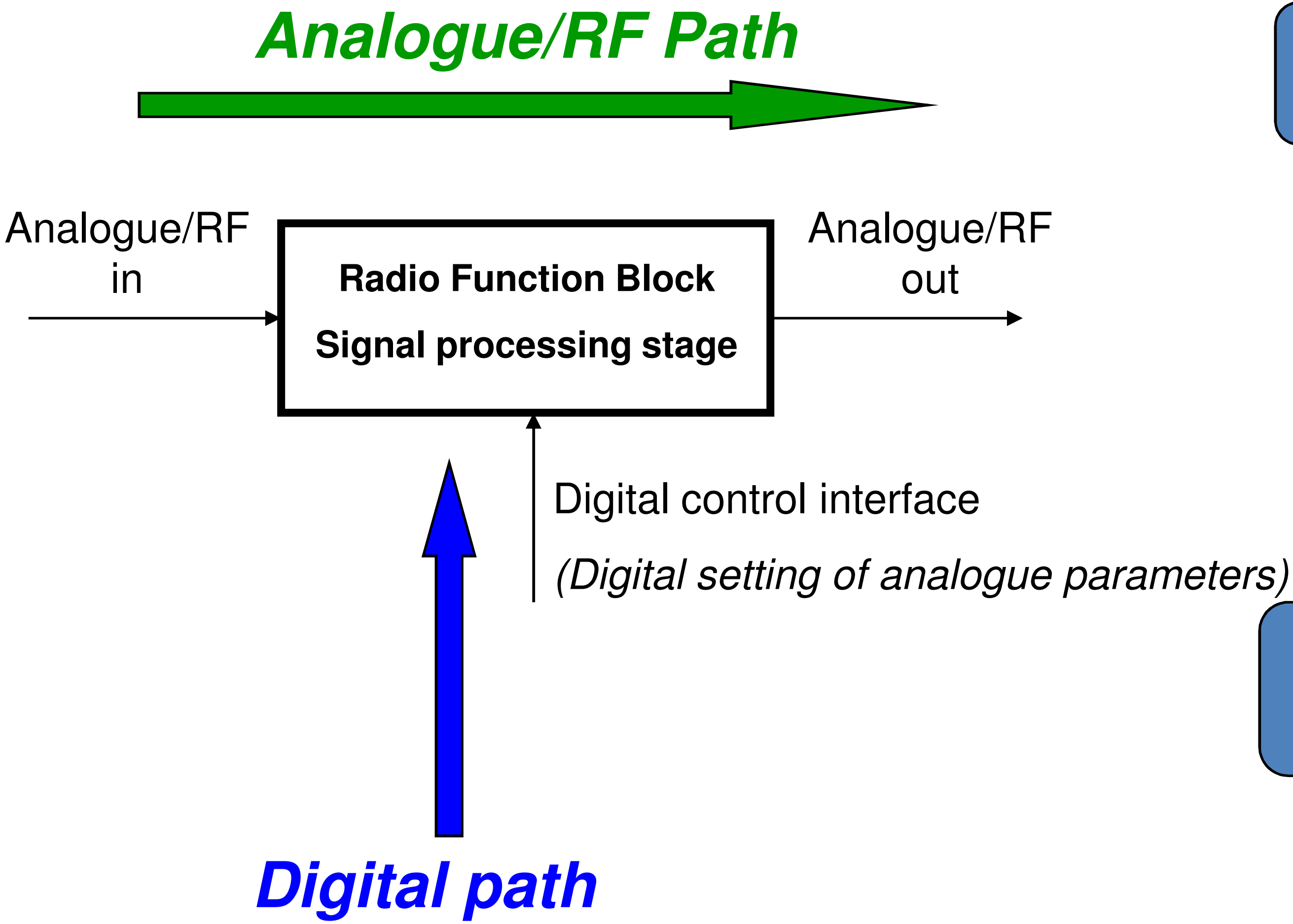
Vision

- Separate processing of AM and PM information
- Delay in AM and PM hasn't to be matched
- EVM makes no sense any longer
- Pulse shaping not in linear domain IQ, but polar domain

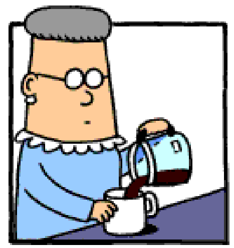
Source: H. Rohling, V. Engels, DIFFERENTIAL AMPLITUDE PHASE SHIFT KEYING (DAPSK) - A NEW MODULATION METHOD FOR DTVB -, International Broadcasting Convention, 14-18 September 1995, Conference Publication No. 413,O IEE 1995.

See also: Cahn C., Combined digital phase and amplitude modulation communication systems, IRE Transactions, communication systems , vol 8, pp. 150-155, ***Sept 1960***

5. Examples



A Renaissance of analogue!

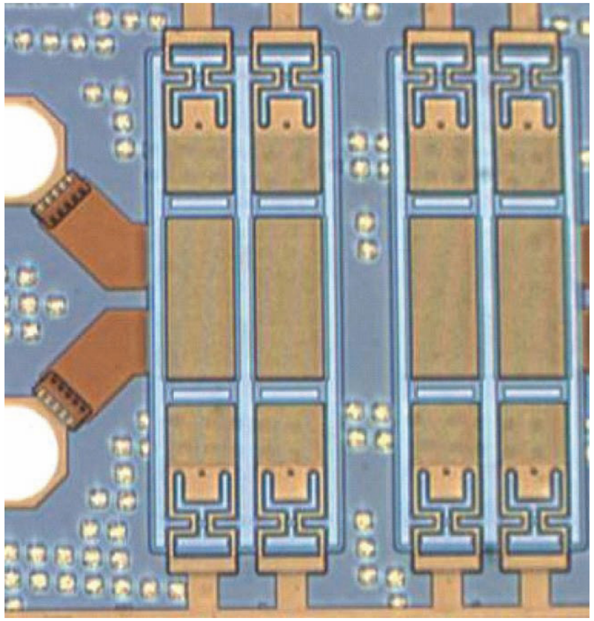


This is a revolution! Software Radio in analogue domain...

This slide is from Oct 2004, my time in Bell Labs

Examples

Digital reconfiguration of analogue functions

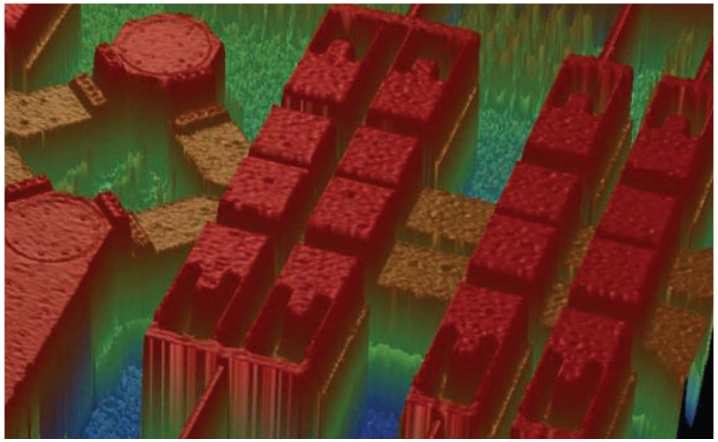


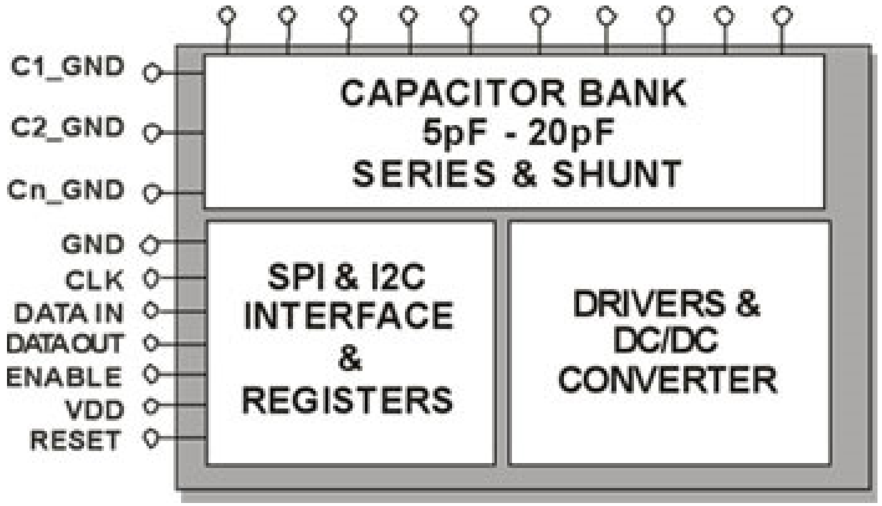
wiSpry

Dynamically Tunable RF

It got reality in 2010
Commercial grade!

MEMS – Tunable Digital Capacitor array (TDCA)

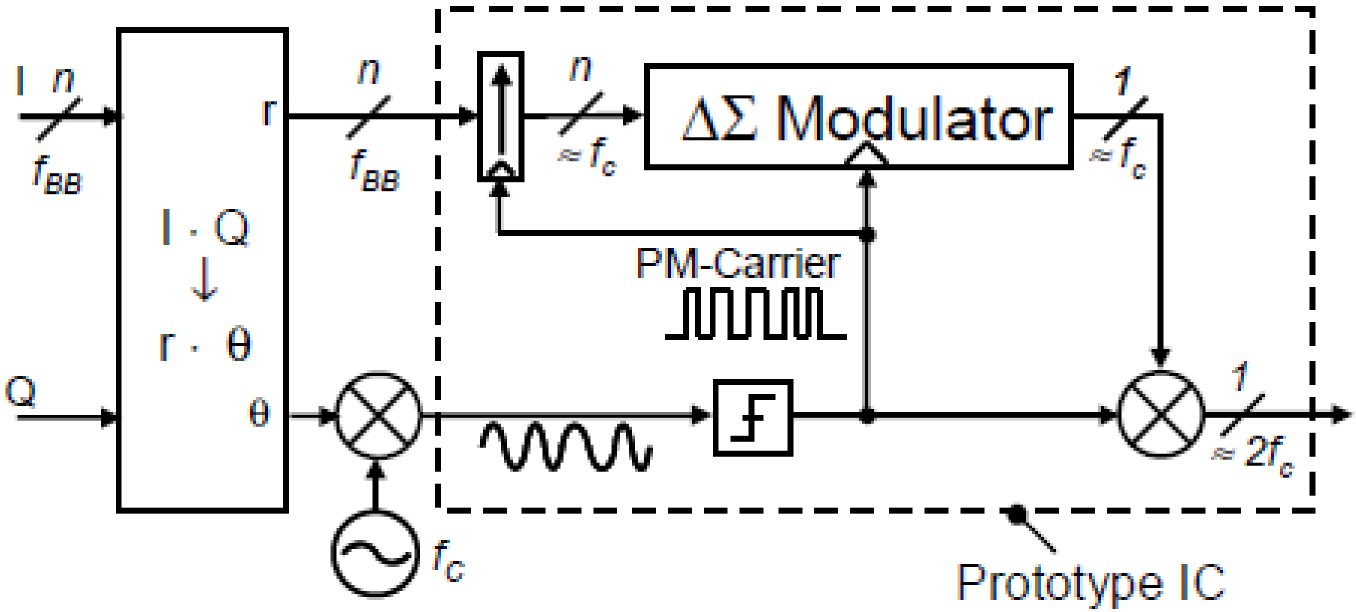




Examples future

Phase modulated clock

(b)



(c)

Source: Shinichi Hori, Kazuaki Kunihiro, Kiyohiko Takahashi, and Muneo Fukaishi, A 0.7-3GHz Envelope ΔΣ Modulator Using Phase Modulated Carrier Clock for Multi-mode/band Switching Amplifiers, IEEE RFIC 2011

Examples future
Phase modulated clock

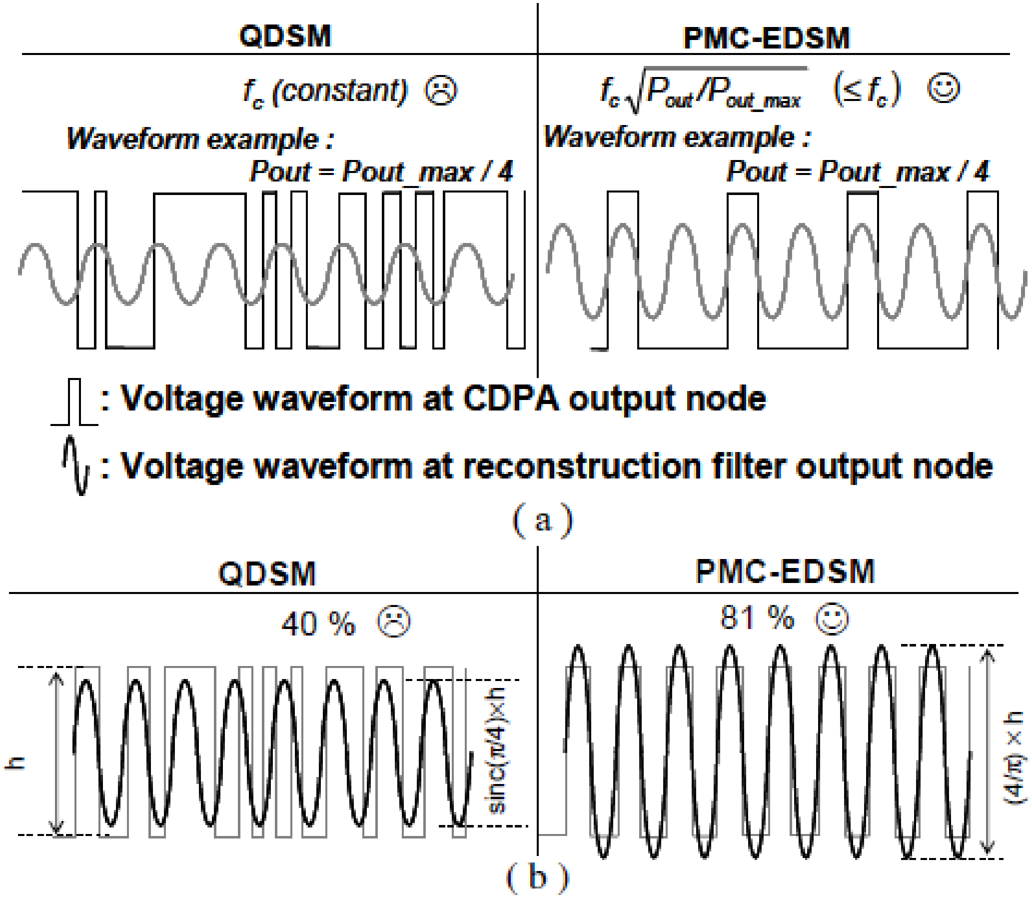


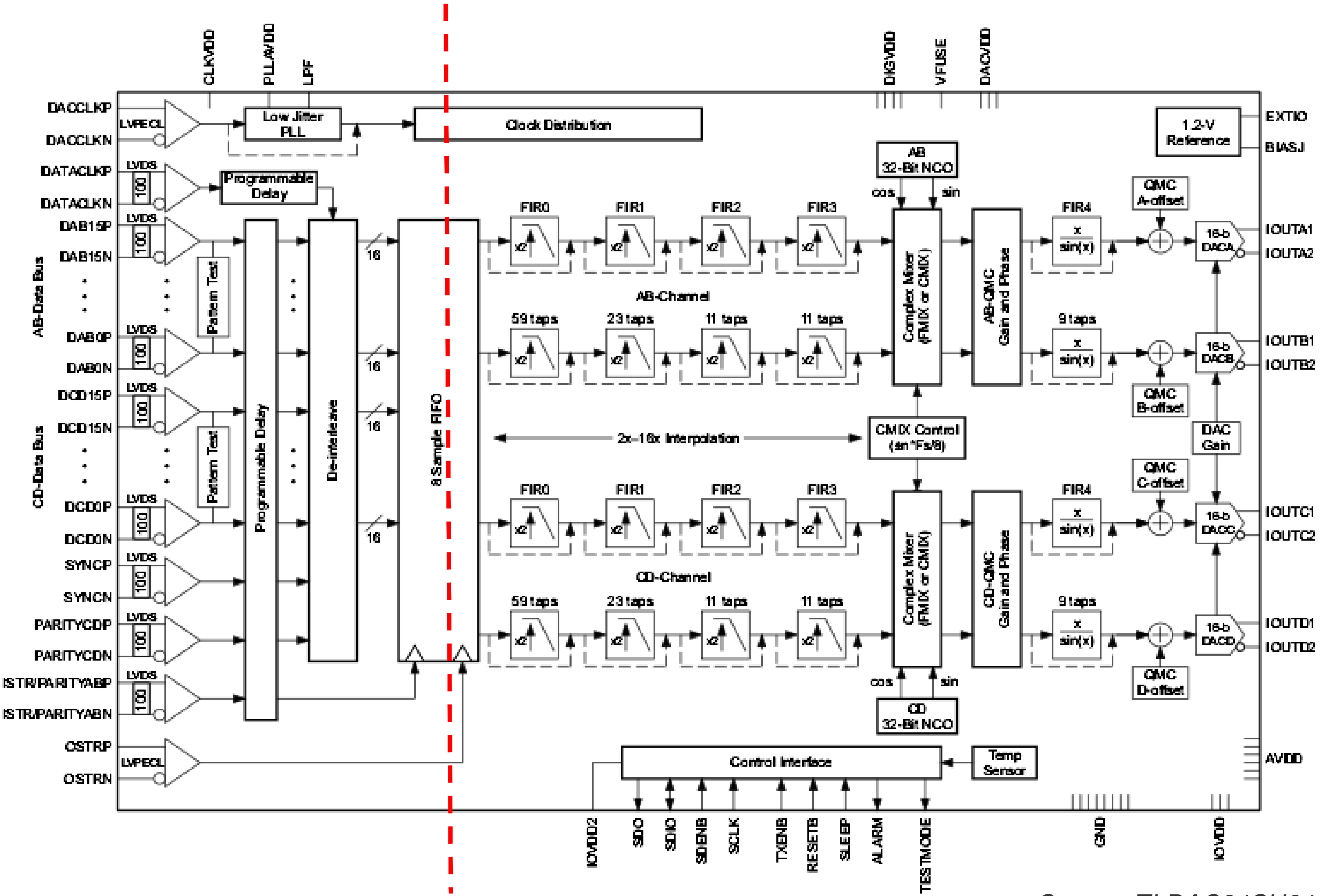
Fig.3 CDPA performance comparison for averaging switching rate (a) and coding efficiency at maximum output power (b)

Time continuous systems perform much better than time discrete ones!

Source: Shinichi Hori, Kazuaki Kunihiro, Kiyohiko Takahashi, and Muneo Fukaishi, A 0.7-3GHz Envelope ΔΣ Modulator Using Phase Modulated Carrier Clock for Multi-mode/band Switching Amplifiers, IEEE RFIC 2011

Examples future

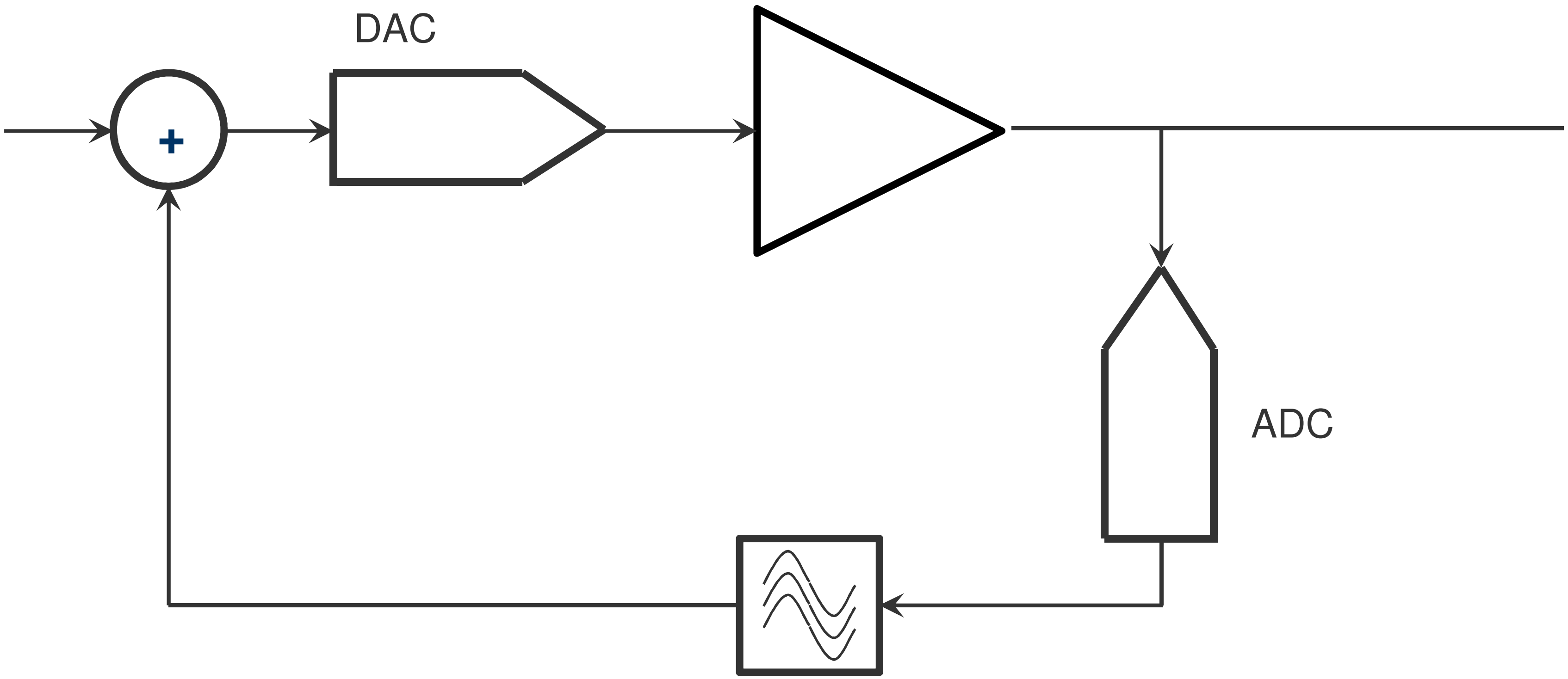
Isolation of clock domains, assynchronous operation



FIFO for separating clock domains

Source: TI DAC34SH84

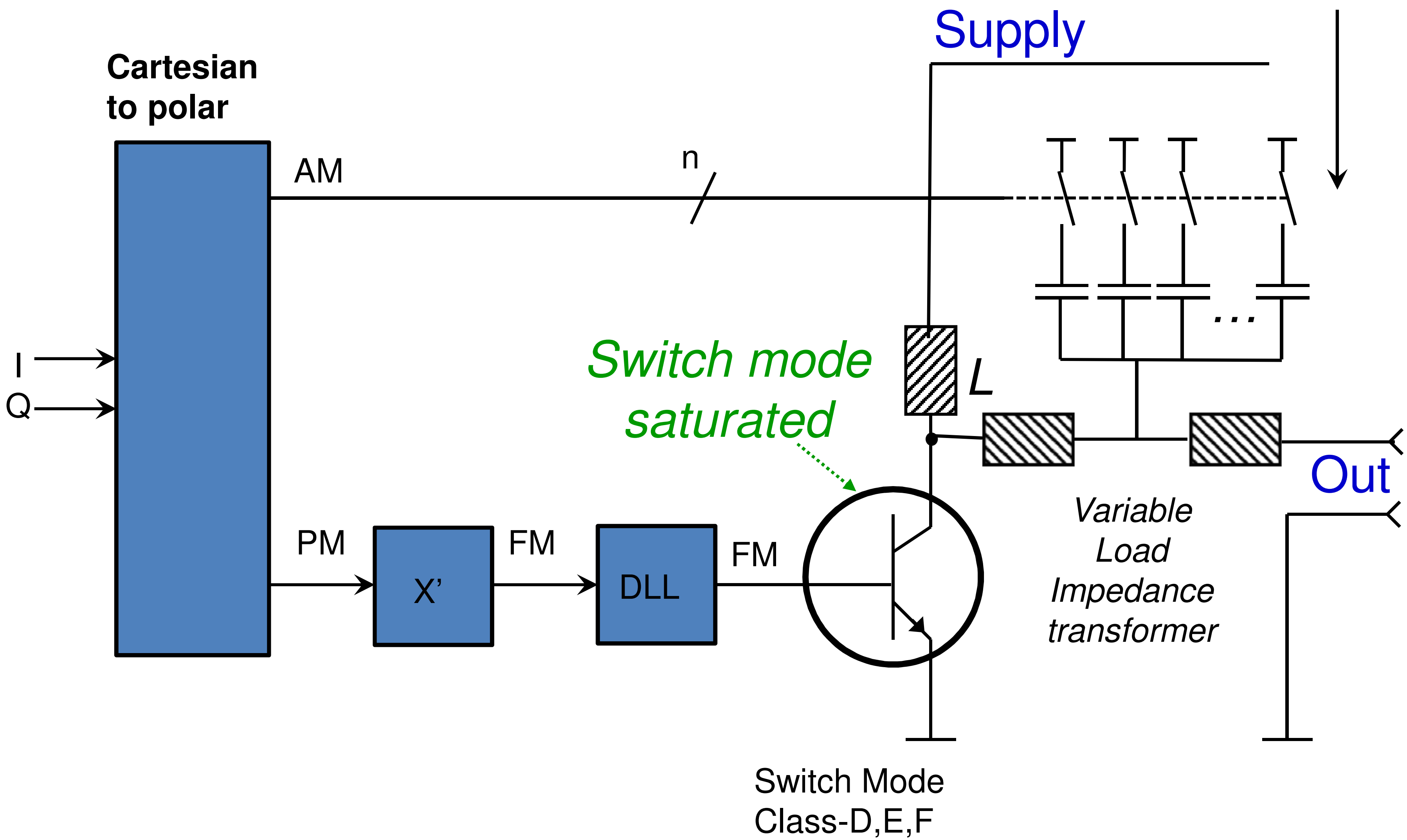
Examples future
Recursive filter



Approach

- Hybrid of analogue and digital processing
- Not a strict analogue recursive filter, nor a digital IIR
- Combine best of both worlds A/D
- Latency of converters critical

Examples future
Discretized passive load modulation



Examples future
Discretized passive load modulation

Implementation constraints

- We cannot strongly attenuate Amplitude
- Can't we define the modulation directly in polar manner?

Requirement

- We need to avoid low amplitudes
- We need a zero crossing free modulation
- We need a modulation with limited PMPR (Peak to minimum power ratio)
- Anyhow we want limited PAPR (Peak to average ratio)

New approach

- Not only focus on clipping = limiting PAPR
- Work on algorithms for PMPR limiting
- GSM EDGE naturally has limited PMPR of 17 dB
- Selected Mapping in OFDM can not only be used for limiting PAPR, but also for limiting PMPR!

6. Conclusion

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Conclusion
Findings

Analogue-Digital Balance

- Analogue is very powerful
- Analogue selectivity always needed
- Knee in sampling rate with converters continuously shifting
- SDR: We cannot shift all to SDR, believing Moore's law

Architecture Innovation is necessary

- 4 quadrants - Beyond Moore
- There is more than just analogue and digital – e.g. PWM, switched cap filter
- New Architectures needed
- E.g. new Filter

Vision

- Modulation format designed to match TRX architecture - Polar definition
- Evolution of PHY and HW realization has to go hand in hand!
- PAPR and PMPR limitation