- DataRace -

Fully Integrated Dual-Polarized Antenna Array with Ultra-Wideband Single-Chip CMOS Receiver

D. Maurath[1], S. Vehring[2] ,B. Deutschmann[3], M.Giese[3], A. F. Jacob[3], G. Böck[2] and F. Gerfers[1],

[1]Technische Universität Berlin, Fachgebiet Mixed-Signal Circuit Design,
[2]Technische Universität Berlin , Fachgebiet Mikrowellentechnik,
[3]Technische Universität Hamburg-Harburg, Institut für Hochfrequenztechnik

friedel.gerfers@tu-berlin.de
datarace@msc.tu-berlin.de

TUHH
Technische Universität Hamburg

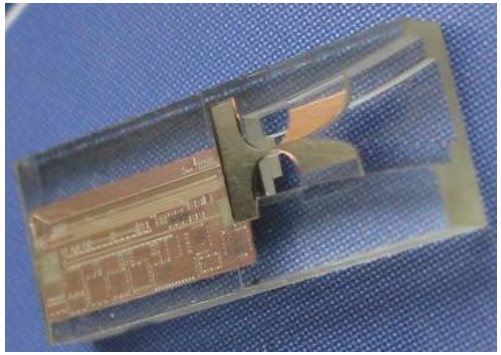
Technische Universität Berlin

Outline

1. **Introduction**
2. SPP 1655 – Project Results
3. SPP 1655/2 – Objectives
4. Conclusions and Outlook

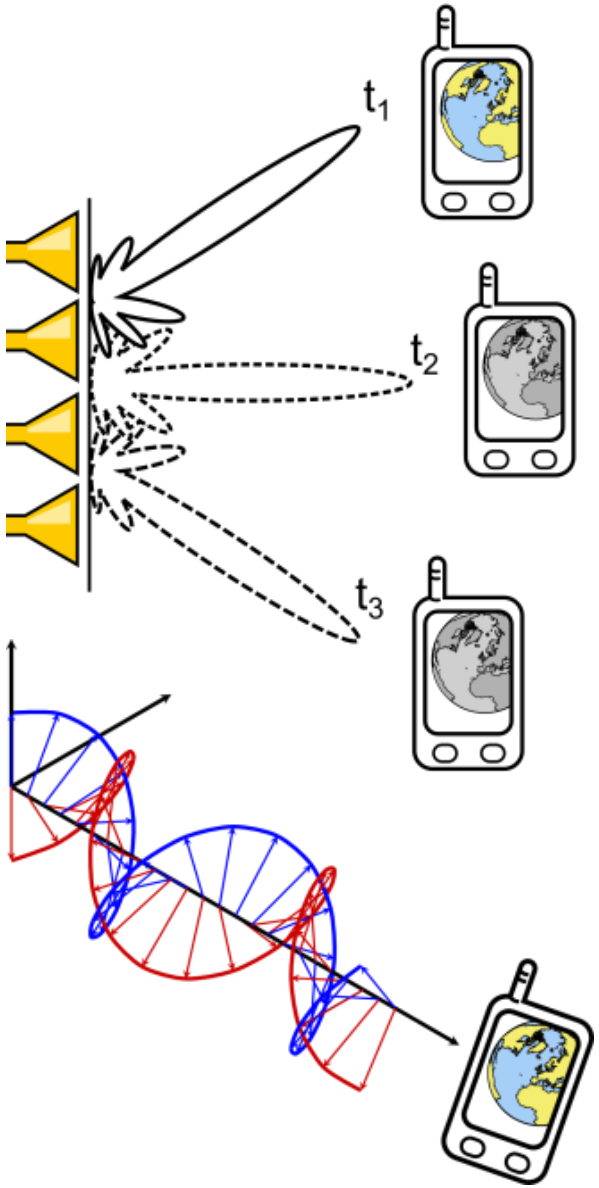
Enabling Technologies for 100 Gb/s

- Low-cost system-in-package
  - Beam-forming system
  - 3D polymer-integrated antenna array
  - Single-chip CMOS transceiver
- Targeting mass-market applications
  - Office-space short-range link (up to 1 m)
  - Video-streaming in airport departure lounges
- Take advantage of entire W-band (75-110 GHz)
  - High relative bandwidth
  - Moderate modulation complexity (moderate SNR)



Array-based Communiction Systems

- Arrays for
  - Free space power combining
  - System scalability
  - 2D Phased arrays / beam steering
- Circular polarization
  - Antenna alignment uncritical
- Dual polarization
  - Double data rate
  - Relaxed link budget requirements



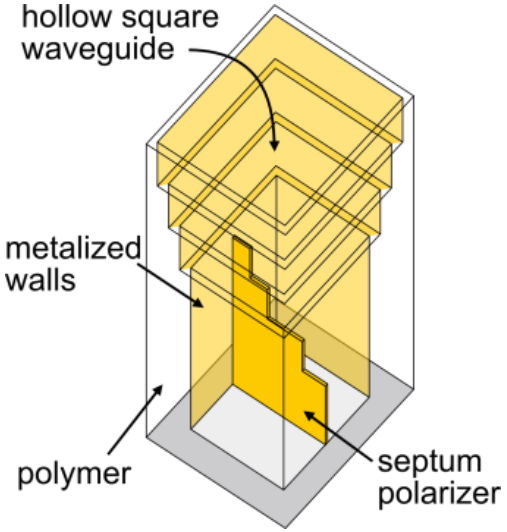
Low-Cost Technologies I

- Polymer process:
  - Vertical growth by polymer deposition and UV-curing
  - Inclined metalized walls
  - Fine resolution (µm scale)
  - Reliable interconnects

Antenna packaging:

- CM: Conventional module
- AiP: Antenna-in-package
- AoC: Antenna-on-chip

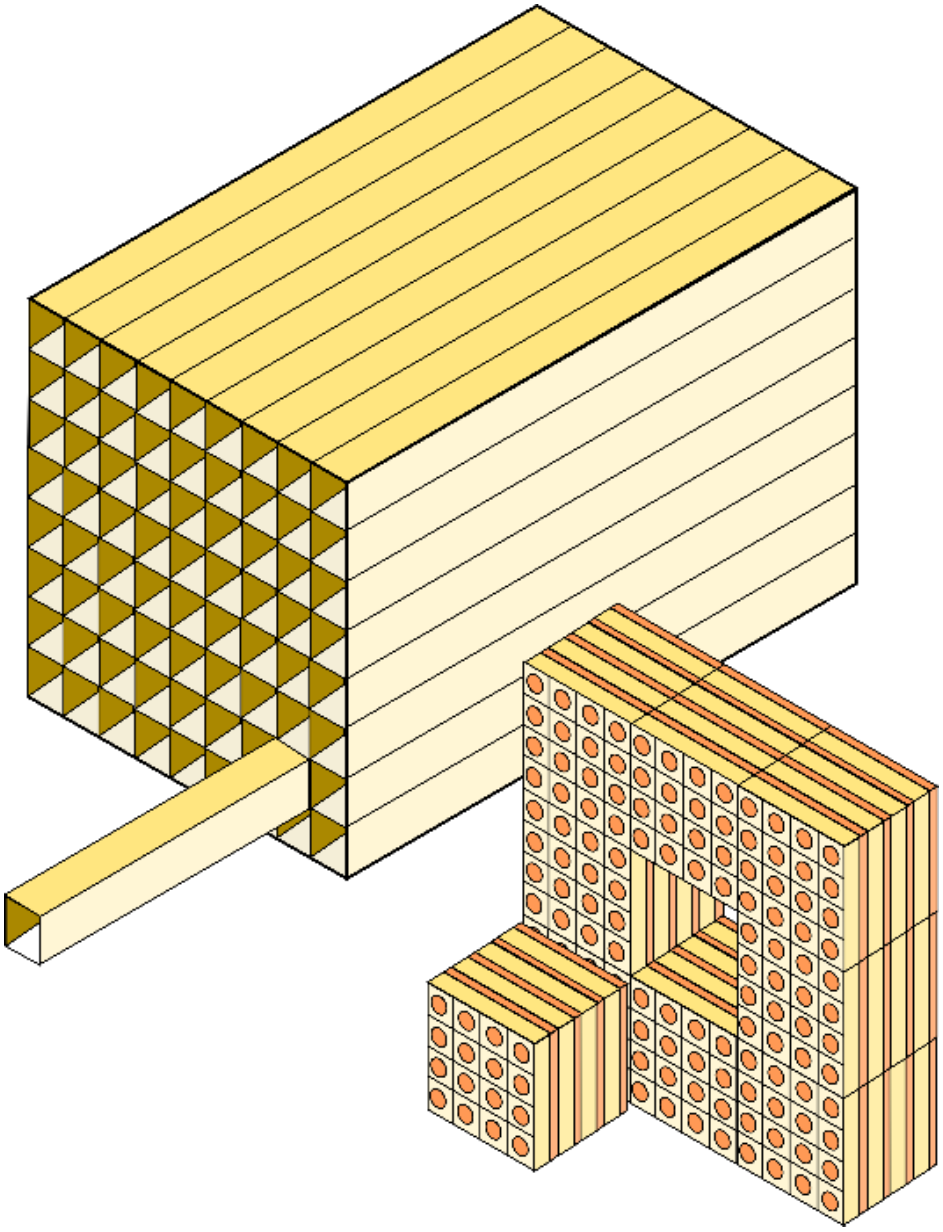
- Antenna-in-package
  - Small chip area even for arrays
  - Improved performance
  - Moderate area consumption
  - Wideband system-in-package up to W-band



[Tripodi et al.]

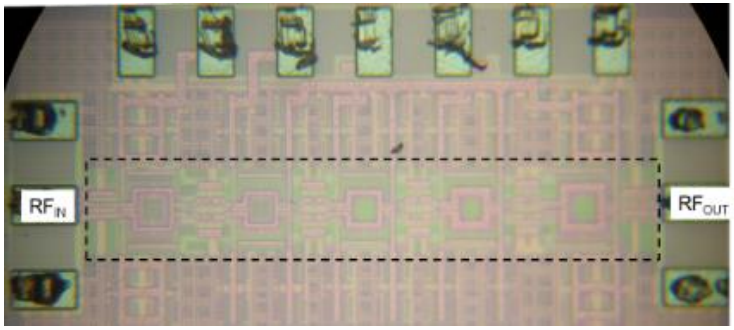
Arrays: Brick vs. Tile

- Brick
  - Simple RF interconnects
  - Scalable to high frequencies
  - Compatible with waveguide
- Tile
  - Layered arrangement
    - Multi-layer PCB process
  - Low thickness



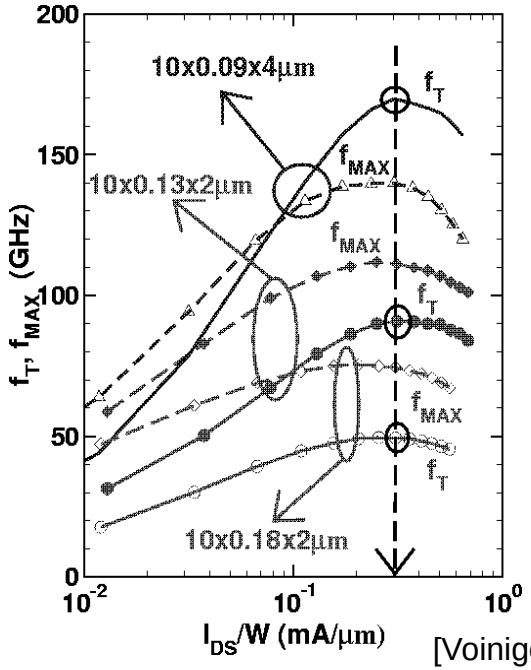
Low-Cost Technologies II

- CMOS technology
  - Highest integration density
  - Mixed signal SoC
  - High reliability
  - Cheap mass production



60 GHz CMOS PA with 0.27 mm^2 chip area

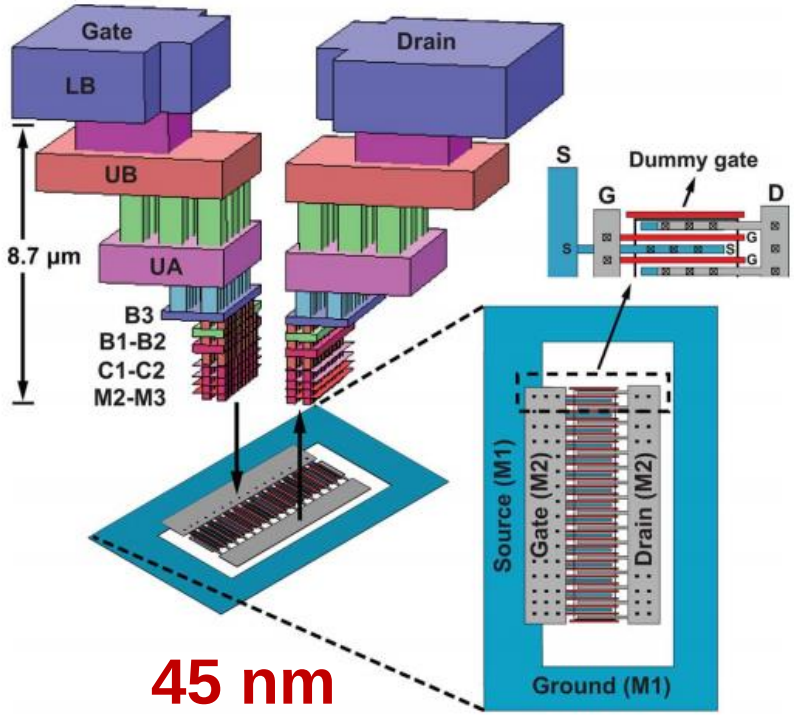
- CMOS gate length downscaling leads to
  - Increasing fT/fmax
  - Lower current consumption
  - Downscaling driven by digital computing
    - Highest integration density
    - Cheap mass production



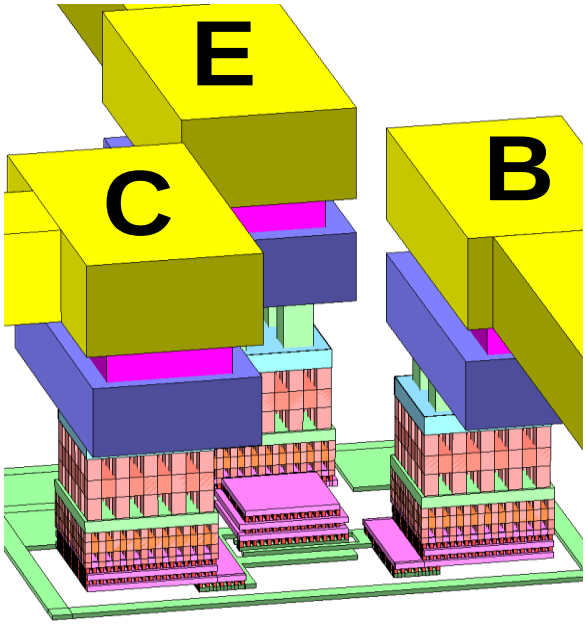
[Voinigescu et al.]

Low-Cost Technologies III

- Nanometer CMOS provides ultra wideband devices (f_{max} & f_T)
- But, we can't build circuits with intrinsic transistors!
- Impact of BEOL parasitics worse in CMOS than SiGe! (2-3 Generations)

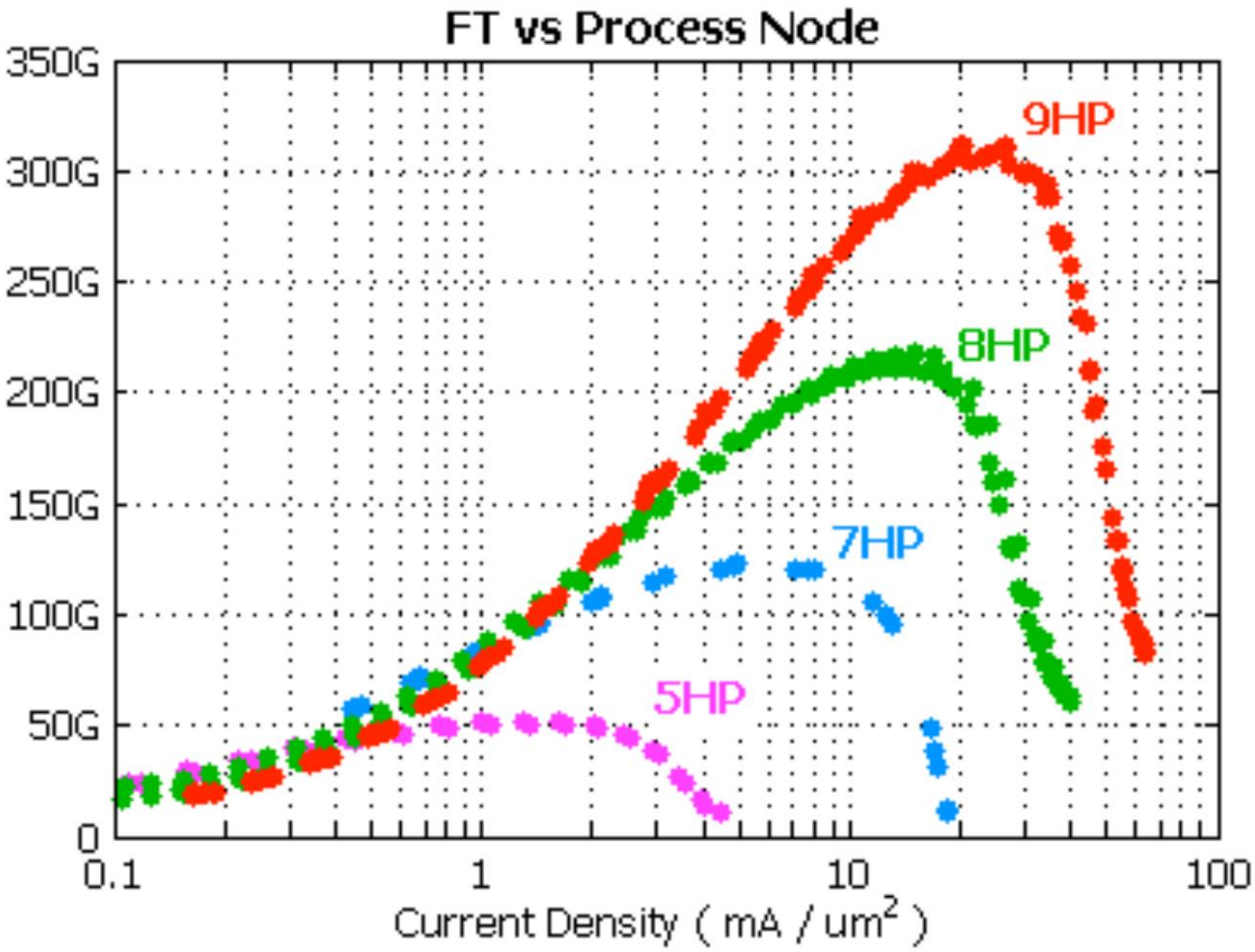


45 nm nFET

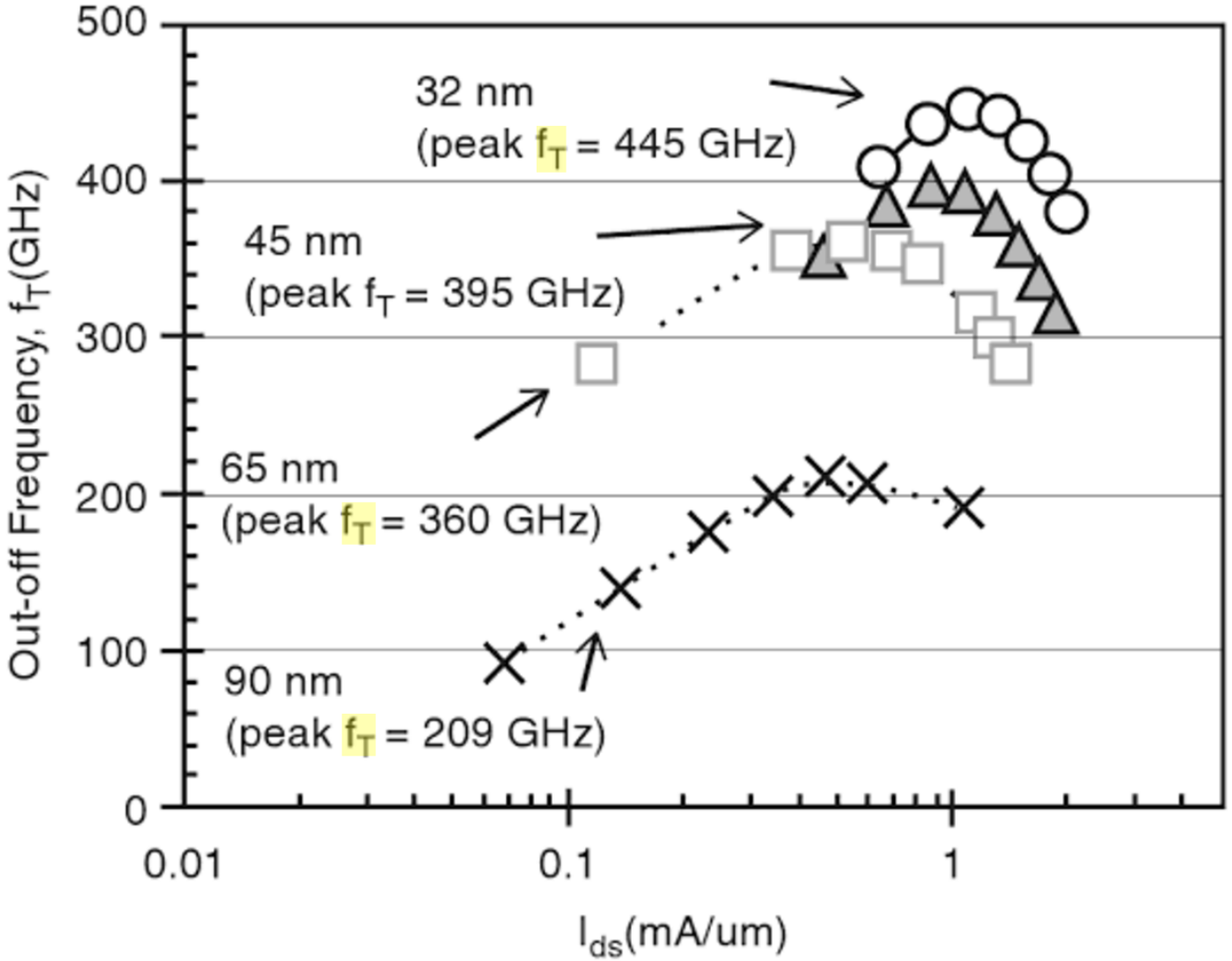


130 nm SiGe HBT

SiGe (IBM) f_T

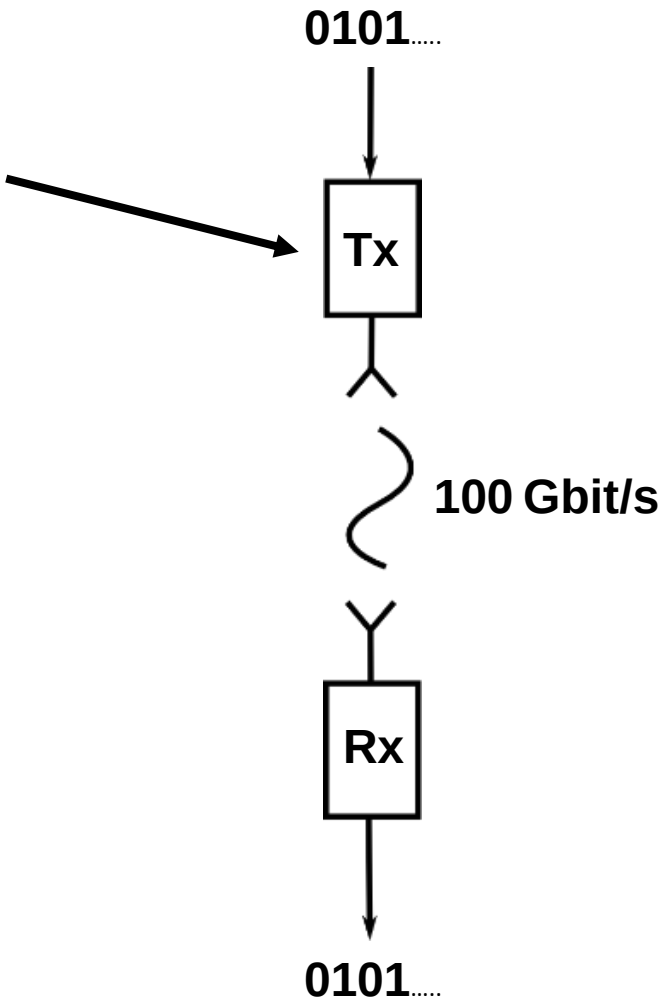

FT vs Process Node
350G
300G
250G
200G
150G
100G
50G
0
0.1
1
10
100
Current Density (mA / um2)
9HP
8HP
7HP
5HP

NFET f_T for nm CMOS Processes

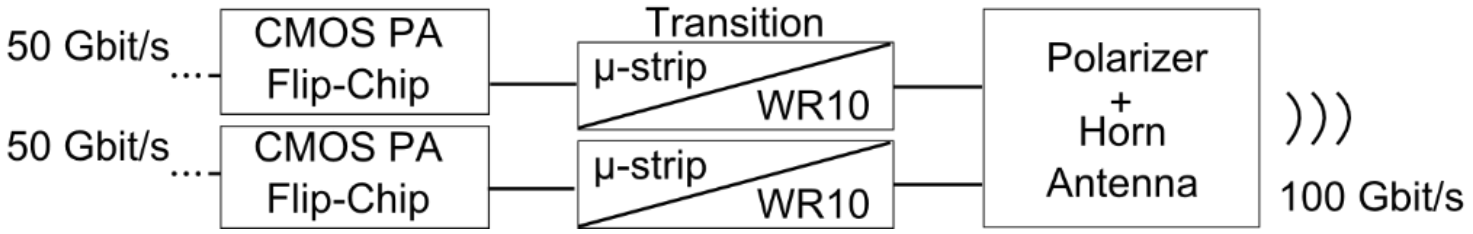


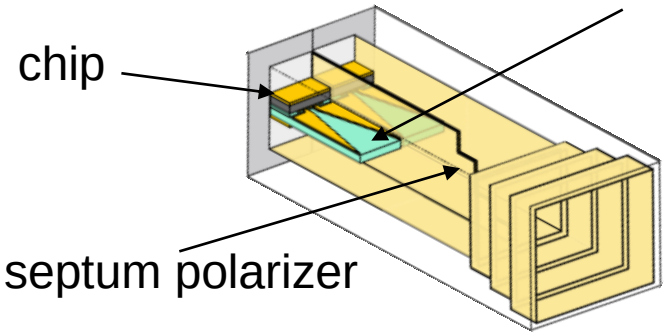
Outline

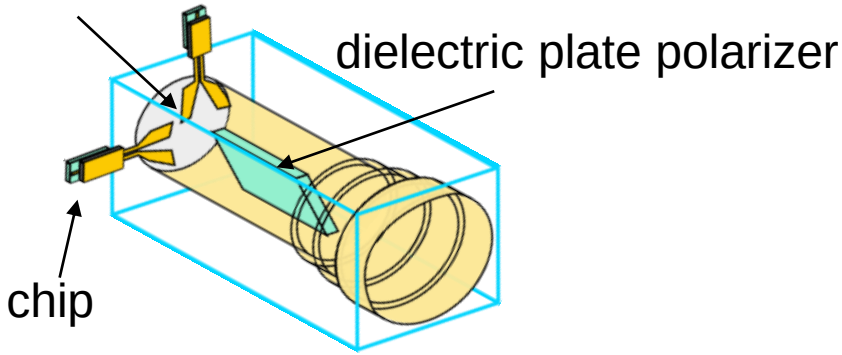
1. Introduction
2. **SPP 1655 – Project Results**
3. SPP 1655/2 – Objectives
4. Conclusions and Outlook



Overall TX Front-End – An Overview







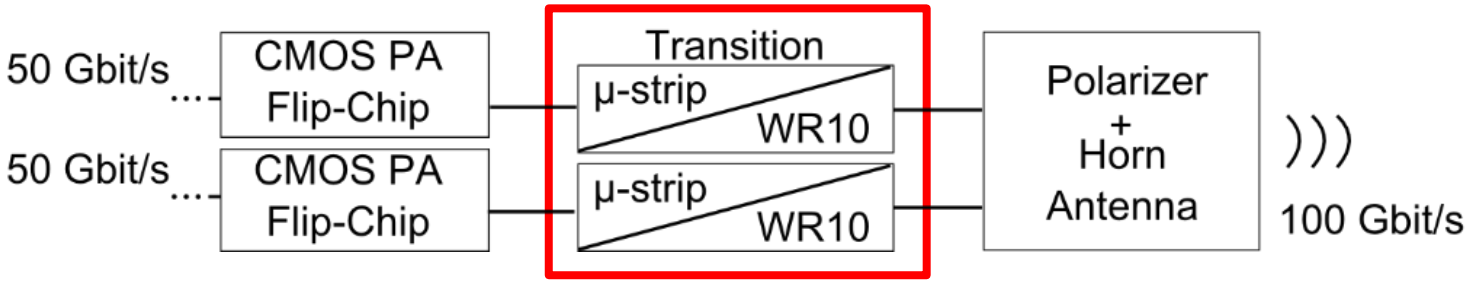
Topology 1

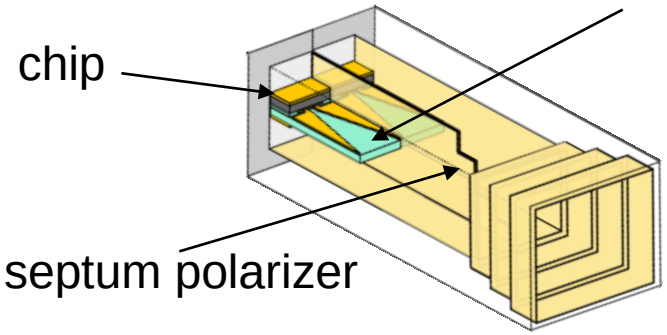
- Inline transition for true brick
- Septum polarizer for compactness

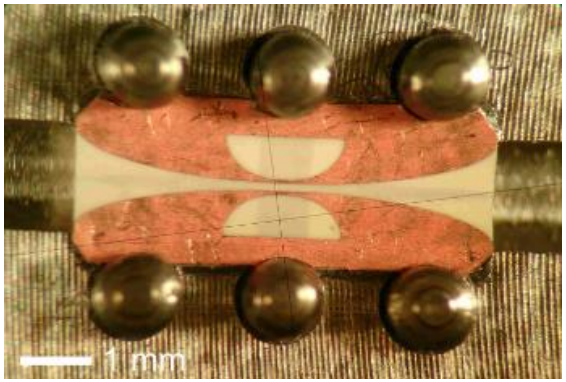
Topology 2

- Vertical transition for dual polarization
- Dielectric plate polarizer for simple setup

Overall TX Front-End - Transition

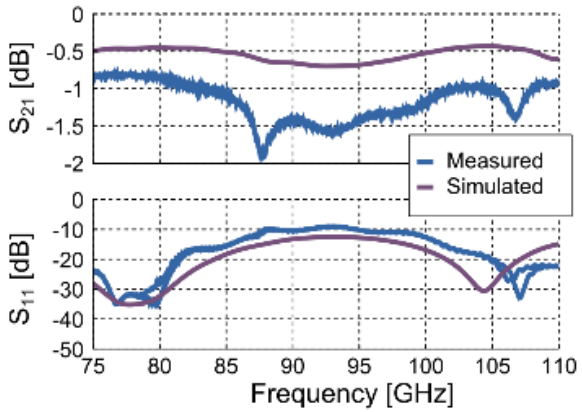






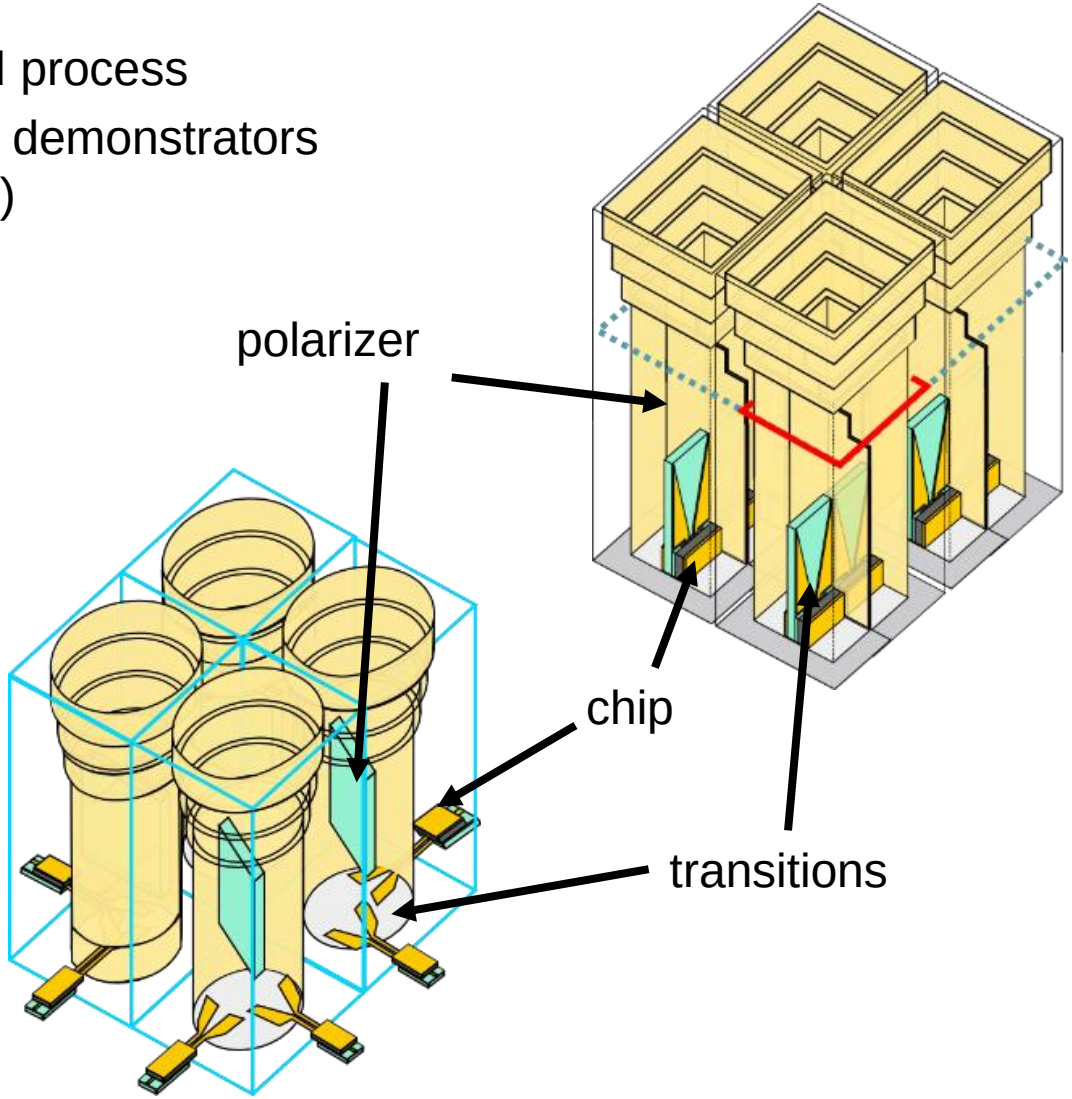
Topology 1

- Inline transition for true brick
- Septum polarizer for compactness



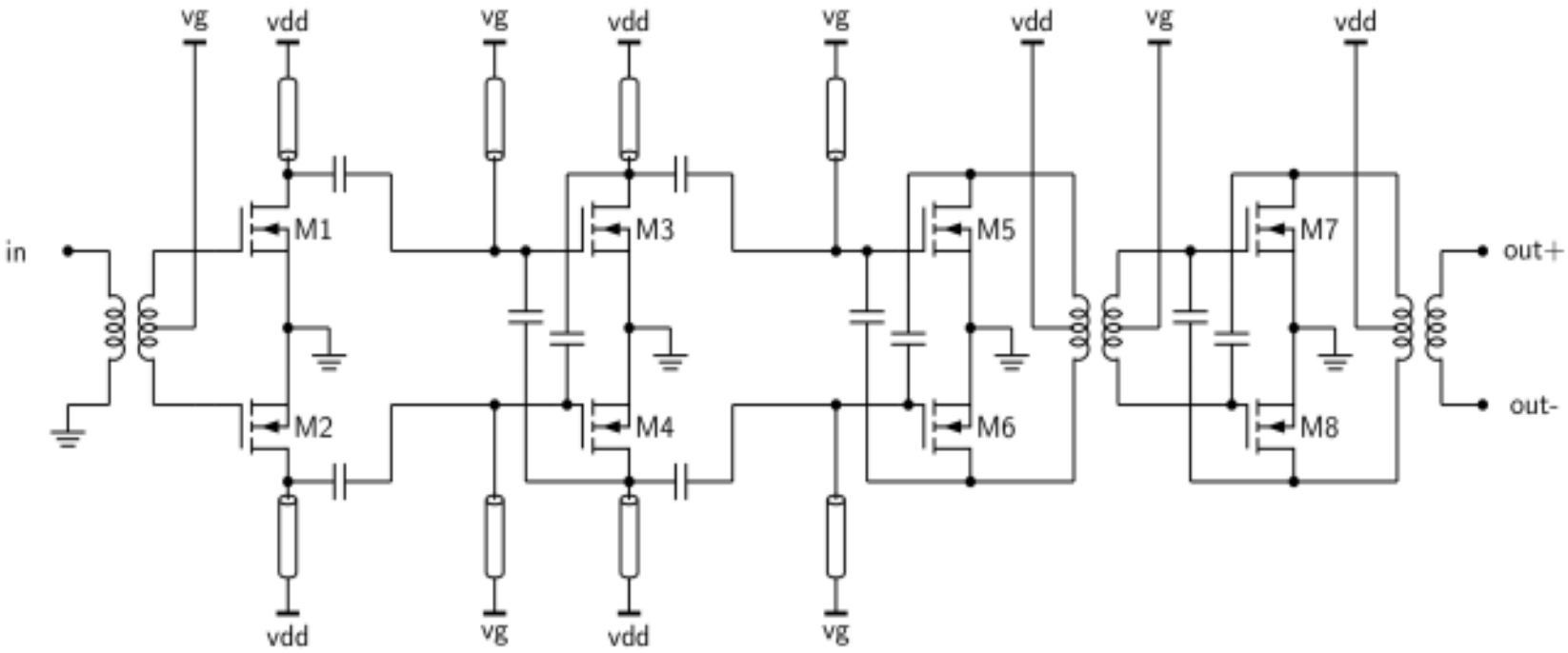
Active Antenna Array for Transmission

- 3D polymer-metal process
- Production of two demonstrators (topology 1 and 2)



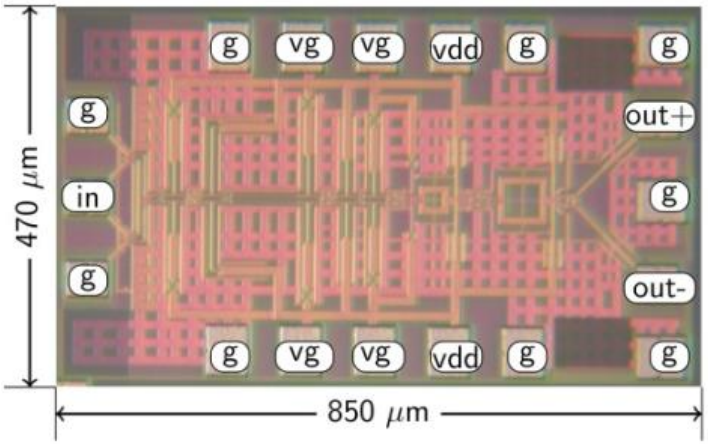
W-Band Power Amplifier Design

- Challenge → Achieve Pout and PAE over 38 % relative bandwidth



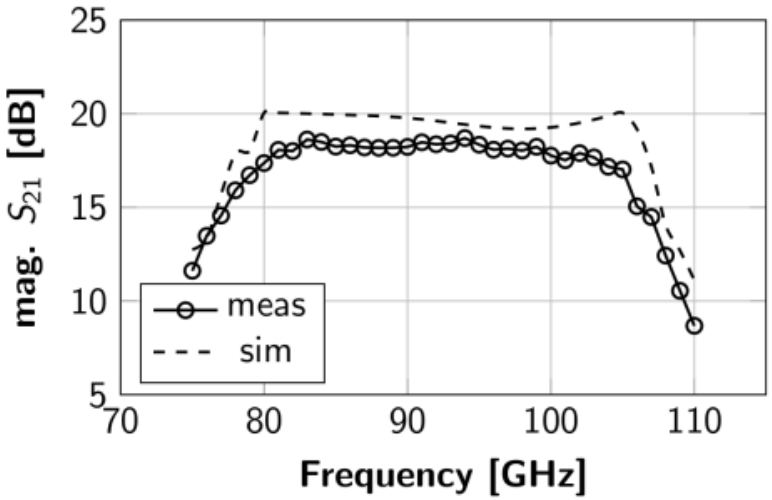
- Features
  - 40 nm CMOS technology, fully differential 4-stage design, neutralized transistors, transformer coupling, broadband matching

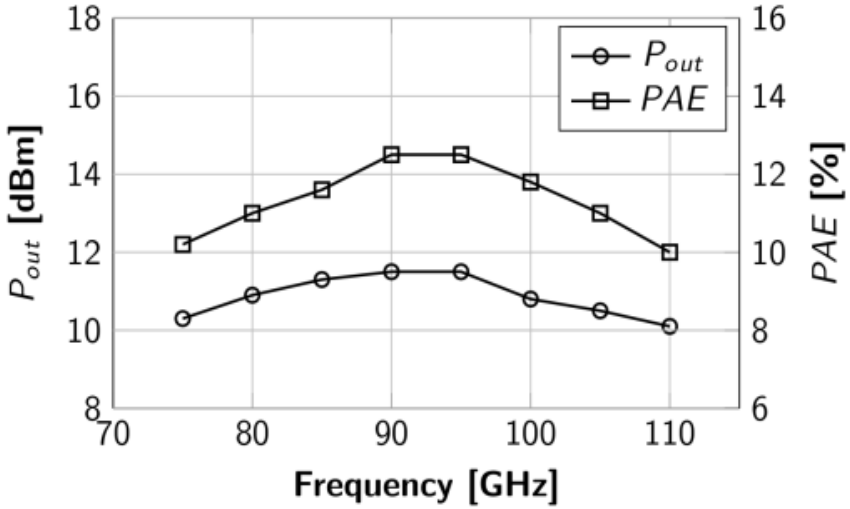
W-Band Power Amplifier Design - Results



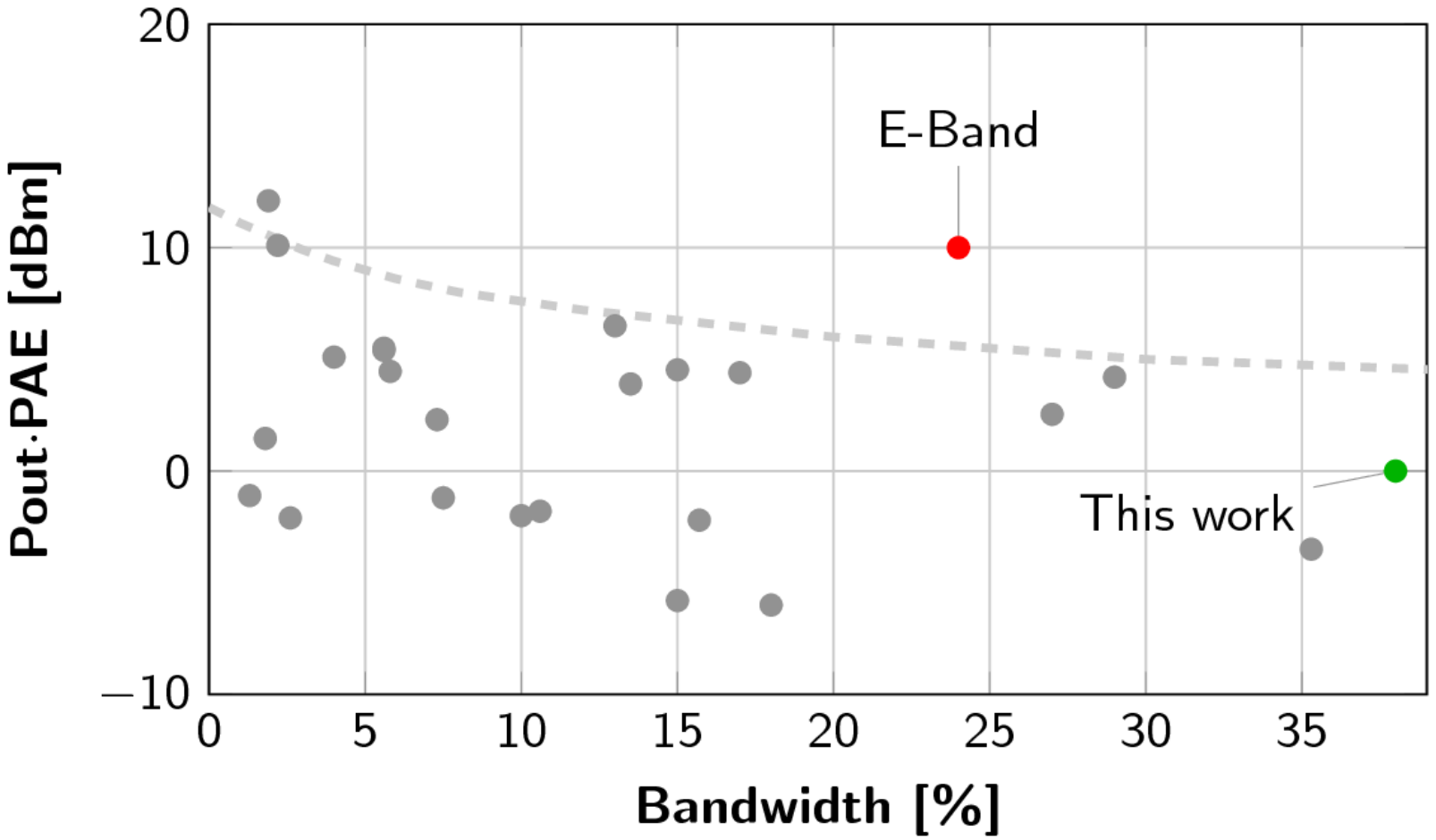
Results

- 18 dB small signal gain
- Pout >10 dBm
- PAE >10 %
- 38 % relative bandwidth
- Good correlation sim/meas.



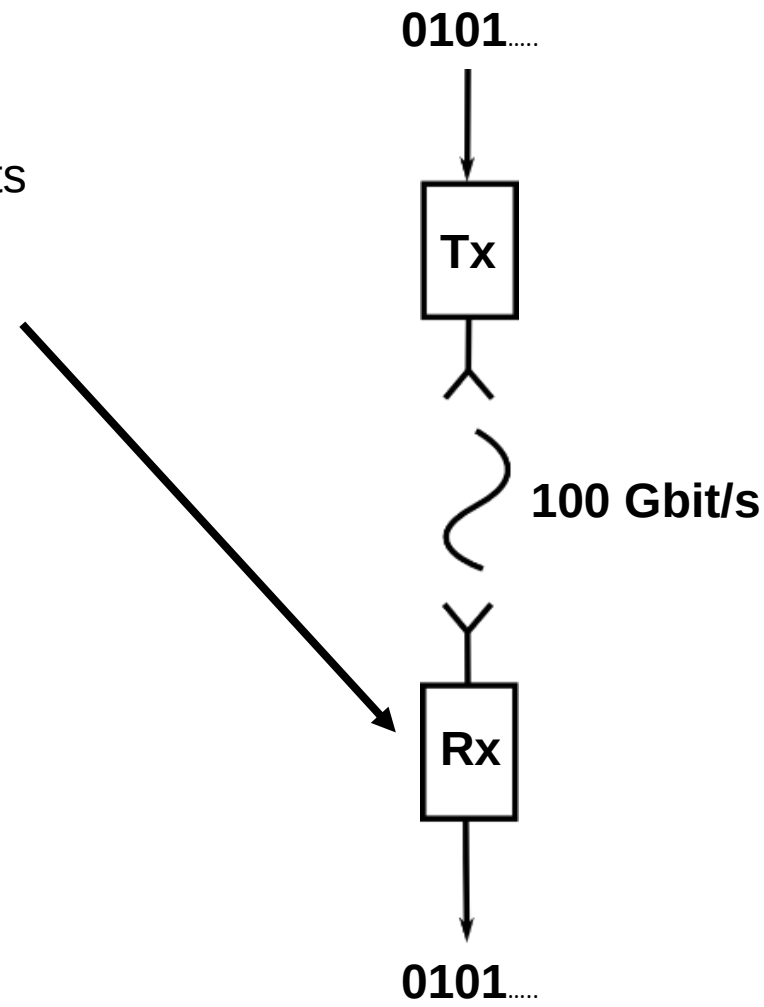


Comparison with state-of-the-art - FOM

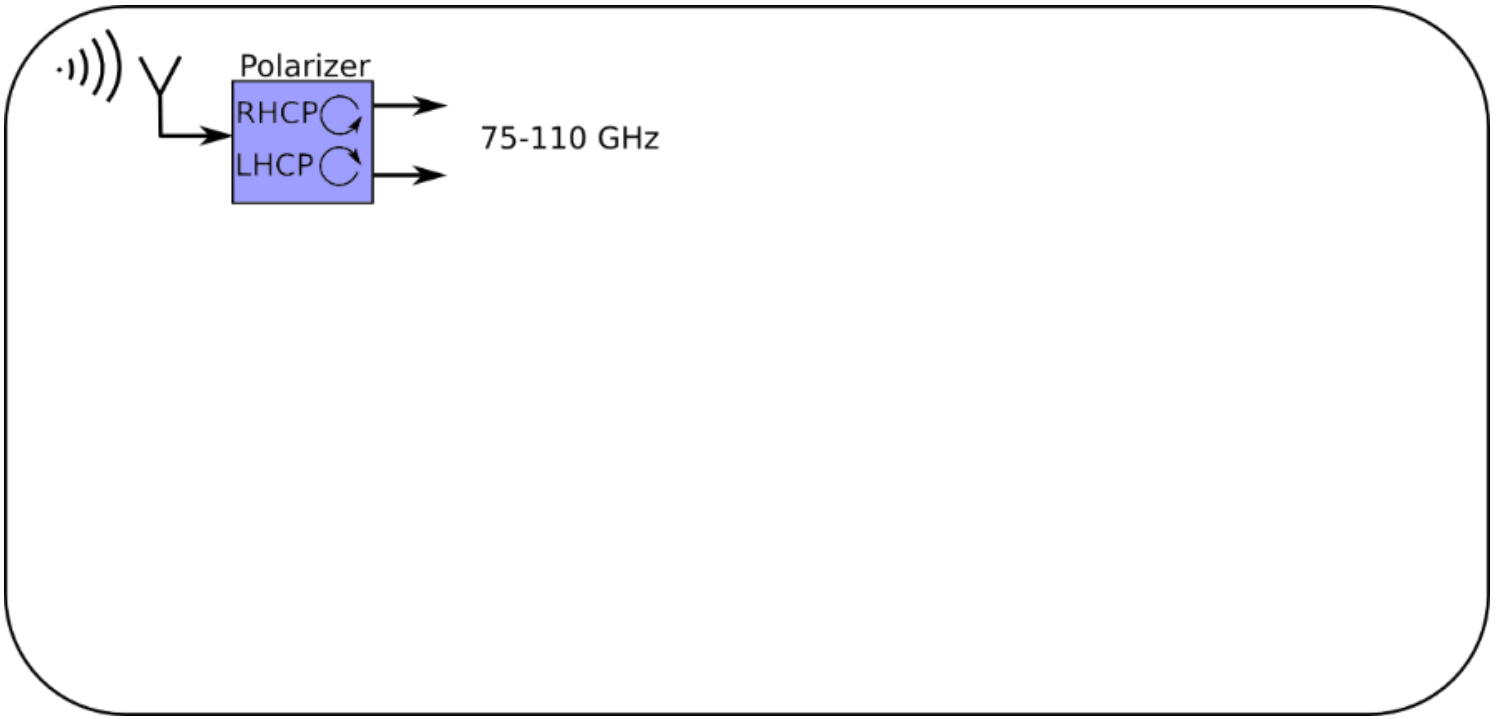


Outline

1. Introduction
2. SPP 1655 – Project Results
3. **SPP 1655/2 – Objectives**
4. Conclusions and Outlook

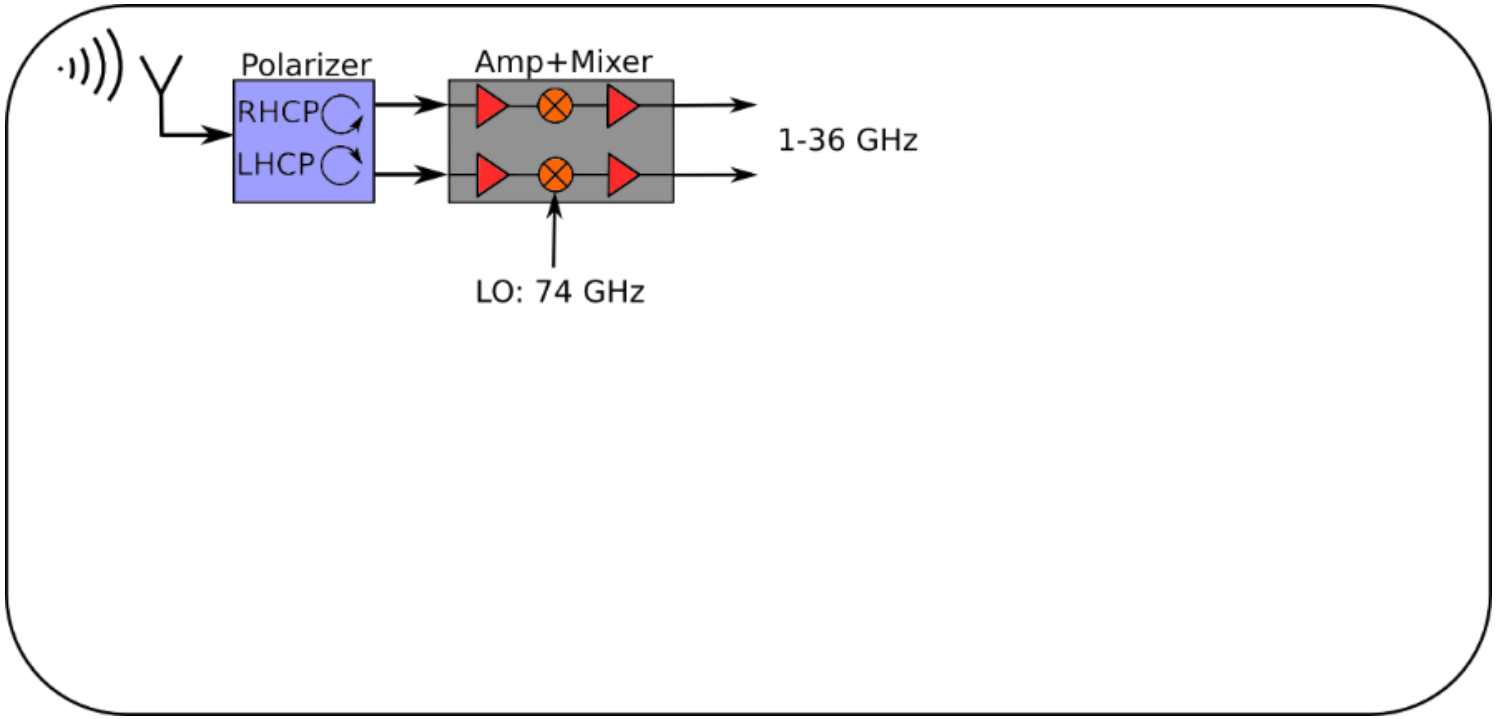


Receiver System



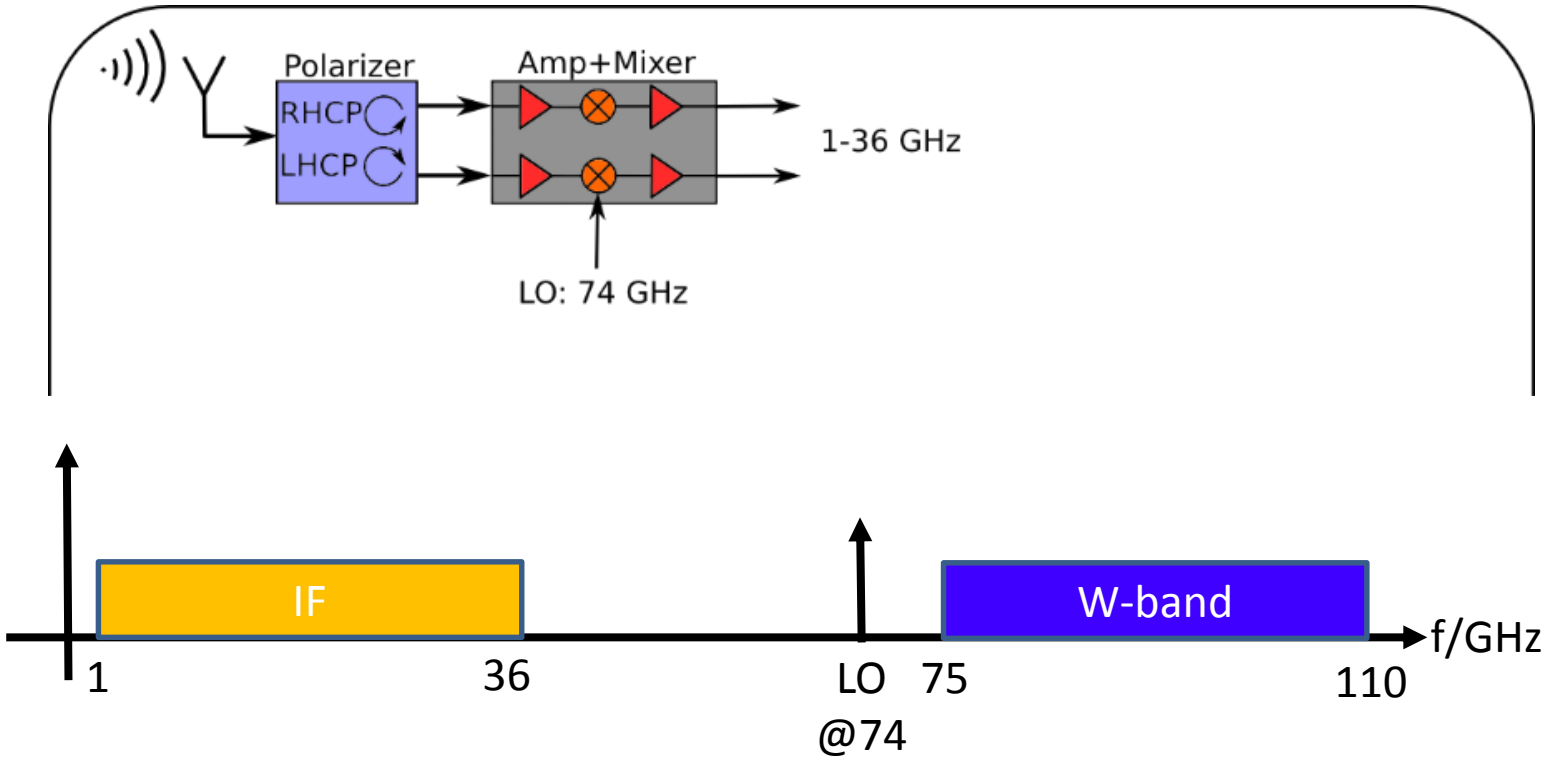
- CMOS chip integration in dual-polarized horn antenna
  - Using 3D polymer-metal process
  - System-in-Package

Receiver System



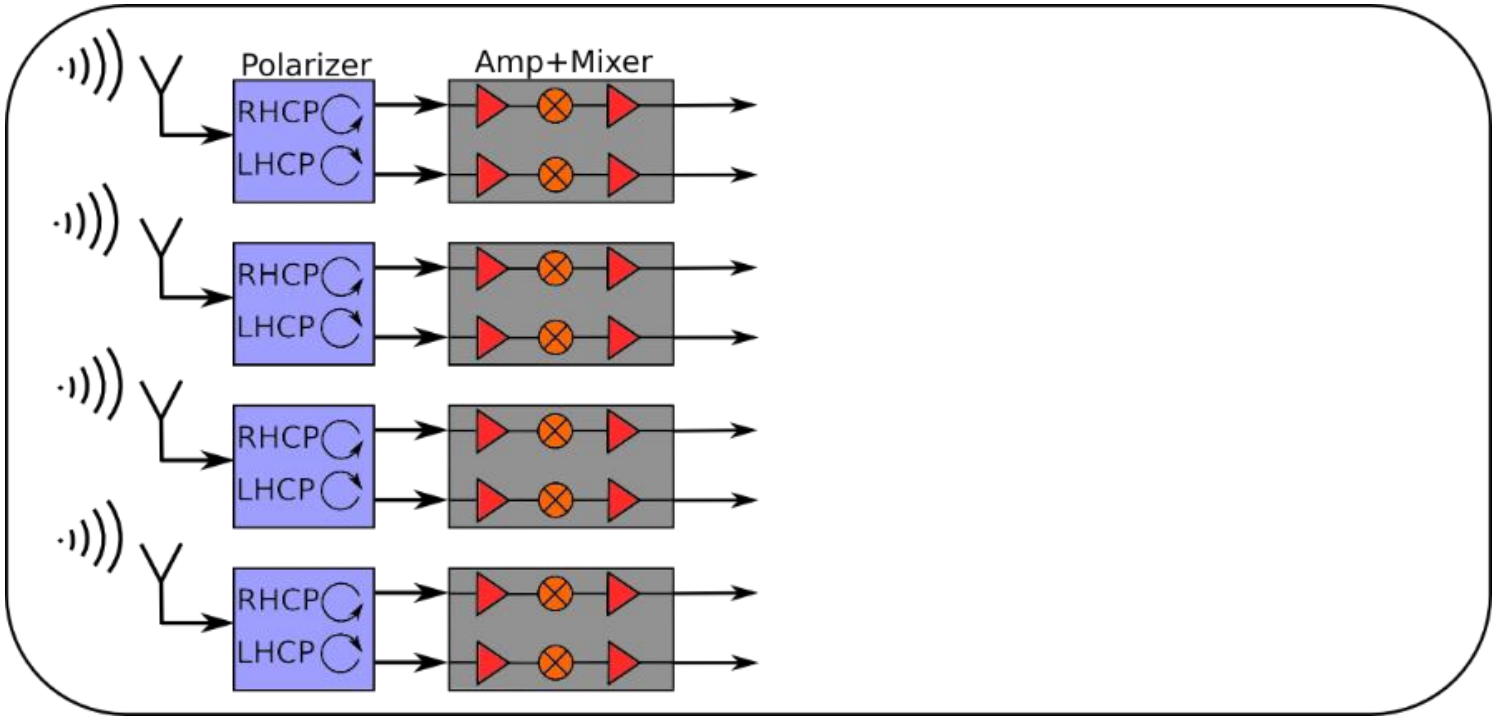
- Single-chip, dual-channel RF-to-digital conversion
- 28 nm high-K metal gate (HPC) CMOS technology
- Full bandwidth low-IF concept (1-36 GHz), no IQ-splitting

Receiver System



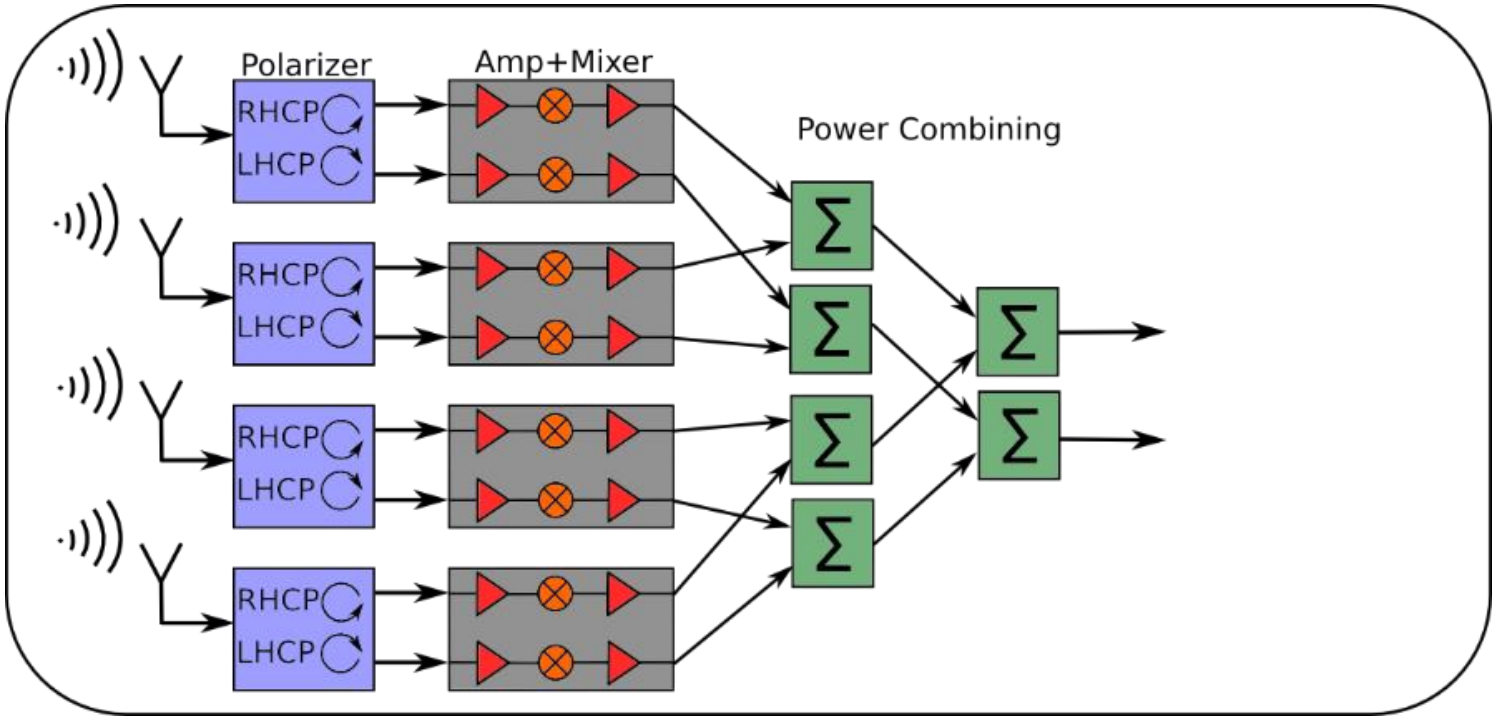
- Single-chip, dual-channel RF-to-digital conversion
- 28 nm high-K metal gate (HPC) CMOS technology
- Full bandwidth low-IF concept (1-36 GHz), no IQ-splitting

Receiver System



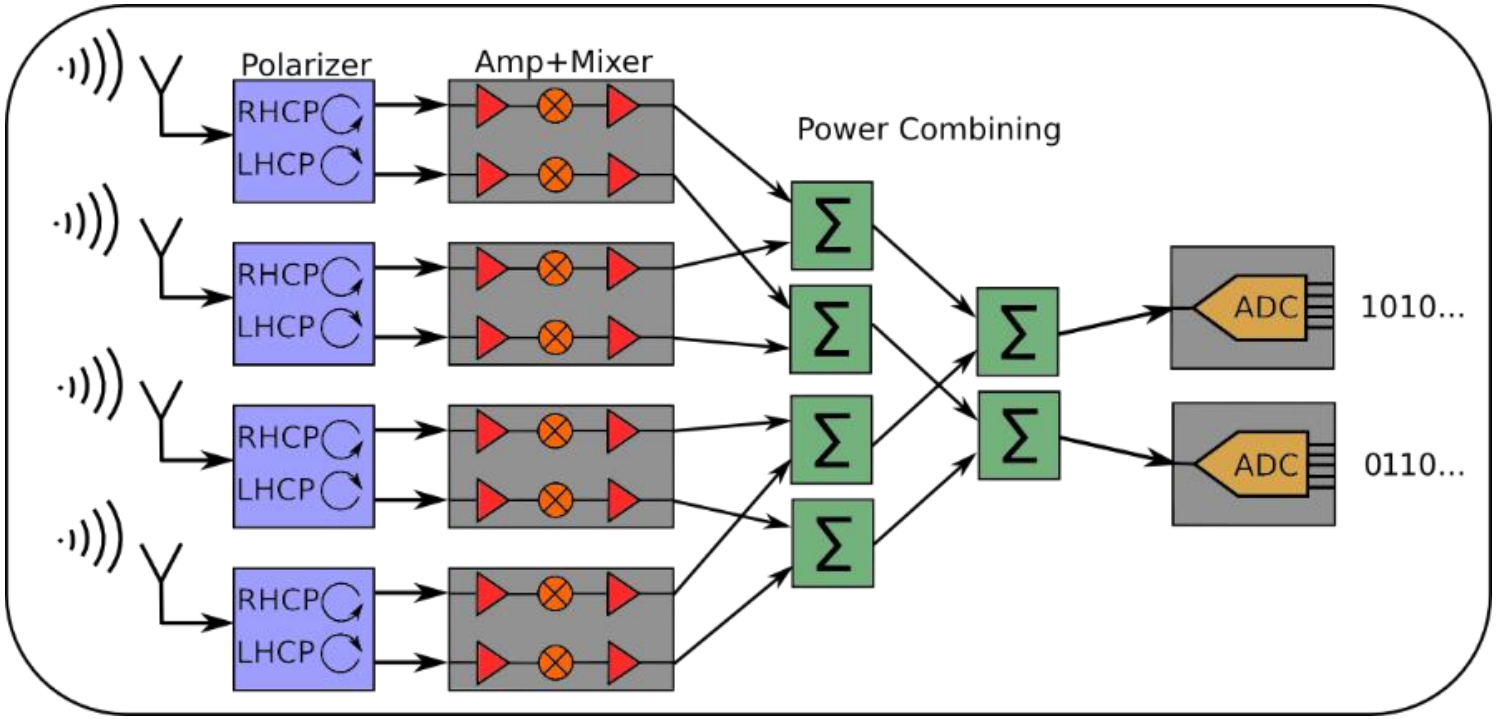
- External LO / clock generation (18 GHz LO to link tests)
  - Two on-chip frequency doubler to 74 GHz
- Beam steering
  - Digital phase shifters

Receiver System



- Power combining at IF
  - Pro: simple
  - Con: channel interference and SNR

Receiver System

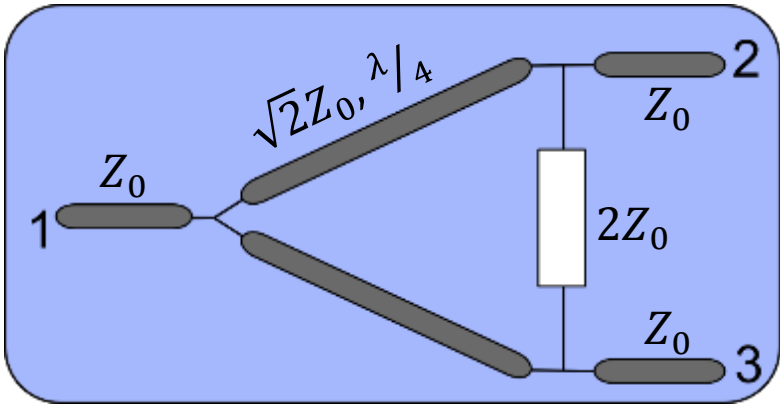


- Impedance-conversion to drive 74 GS/s T&H
- 74 GS/s (time-interleaved) ADC
- 5 bit ENOB
- RF-to-Digital outputs (➔ decimated output or on-chip memory)

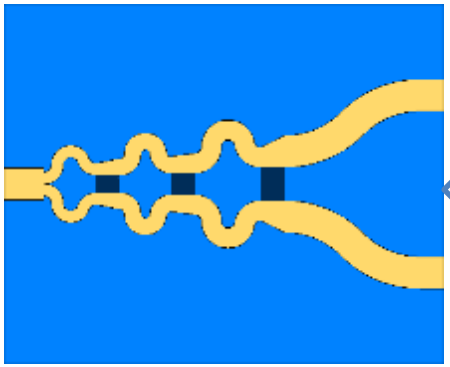
Receiver-Topology - Power Combiner

Wilkinson power combiner

- Limited bandwidth
  - Multiple sections
- Lumped element resistor needed
  - Film-resistors with less parasitics

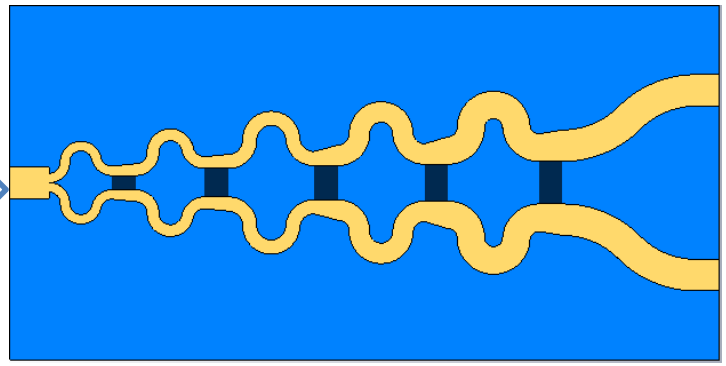


3-Steps

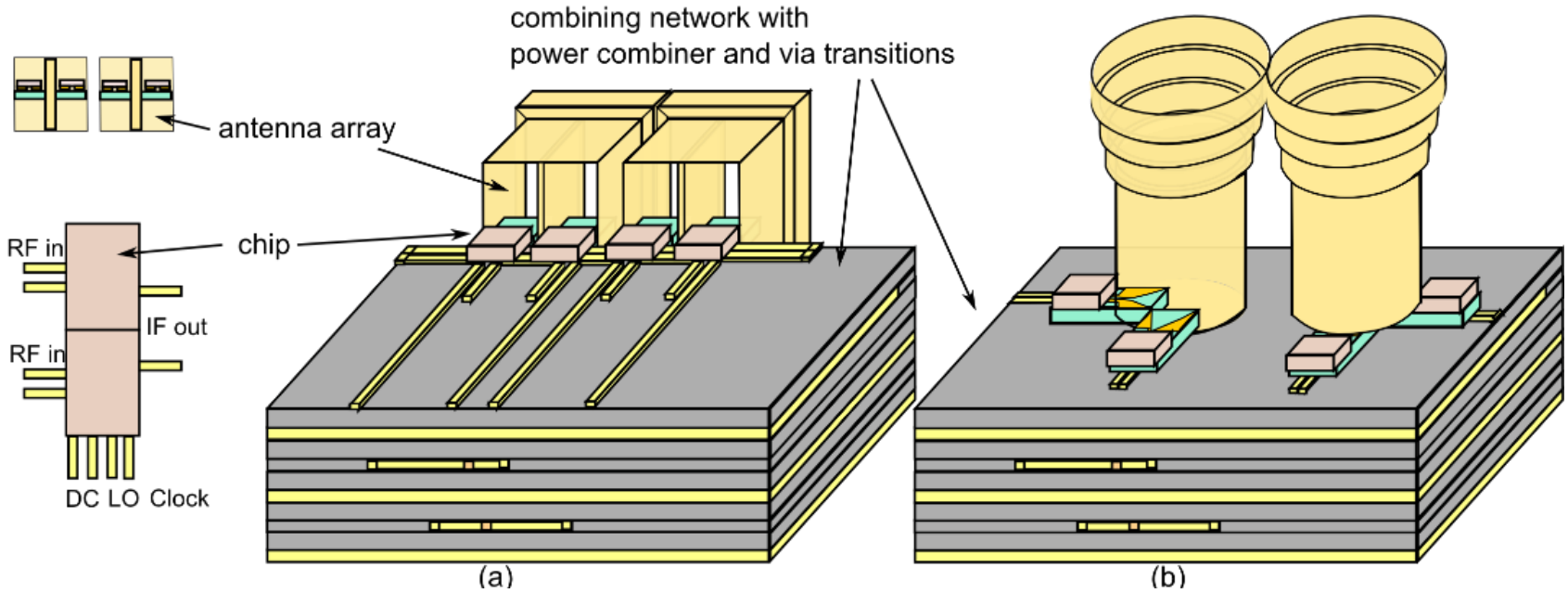


Losses vs. Bandwidth

5-Steps



Receiver-Topology - Antenna Array I

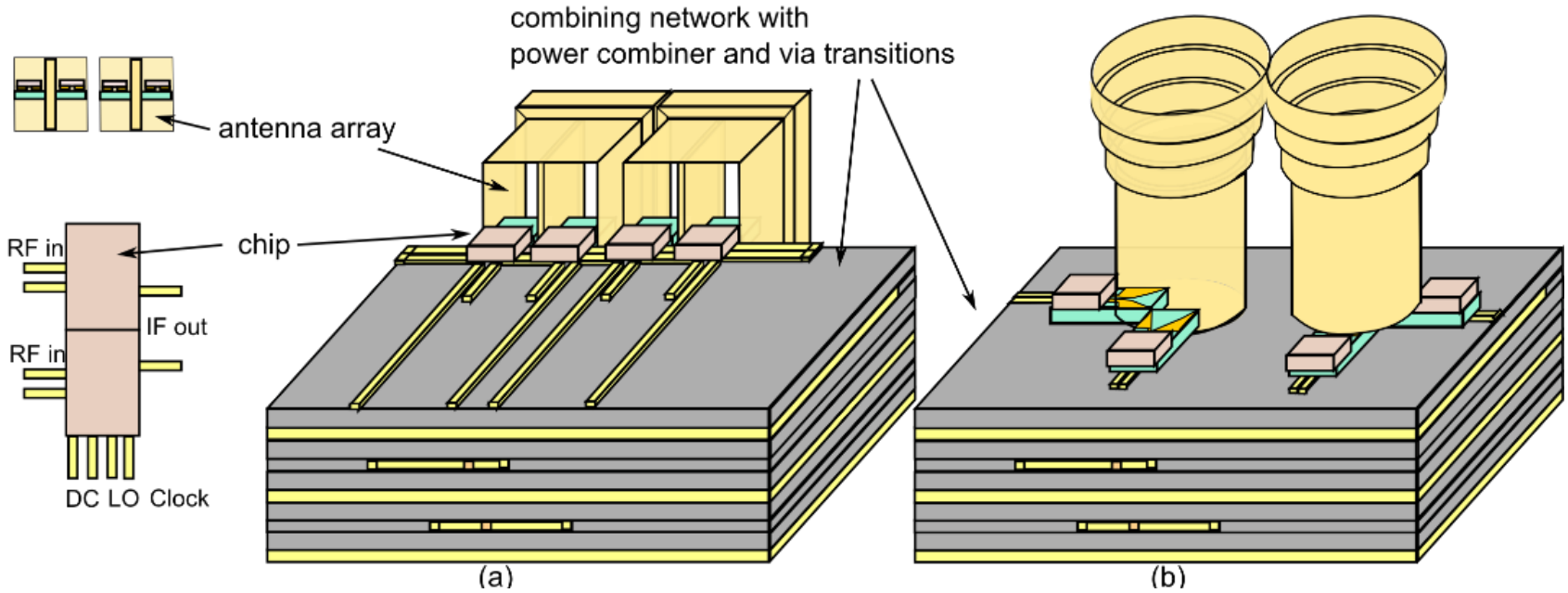


Brick-Type Arrangement **Hybrid Tile Arrangement**

Multi-layer feed network

- Monolithic integration
- 3D polymer-metal process
- LO distribution network and ADC on separate motherboard

Receiver-Topology - Antenna Array II



Brick-Type Arrangement

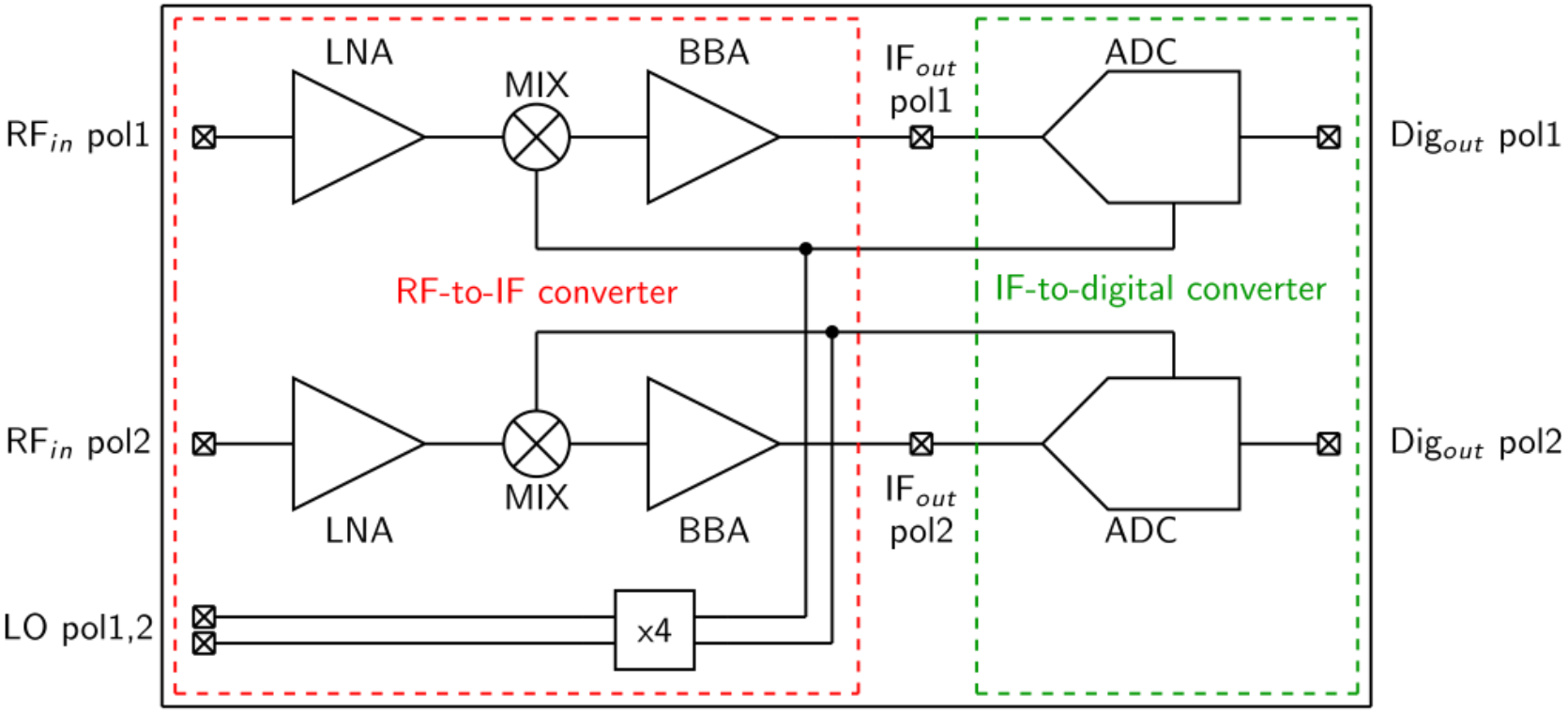
- Feed network in line w/ front-end
- Antenna rows
- Grown layer-wise
- Interconnected on motherboard
- Land- or ball-grid for 2nd level interconnects

Hybrid Tile Arrangement

- Tile architecture for feed network
- Vertical growth
- Integrated layer interconnect
- Full monolithic 3D integration

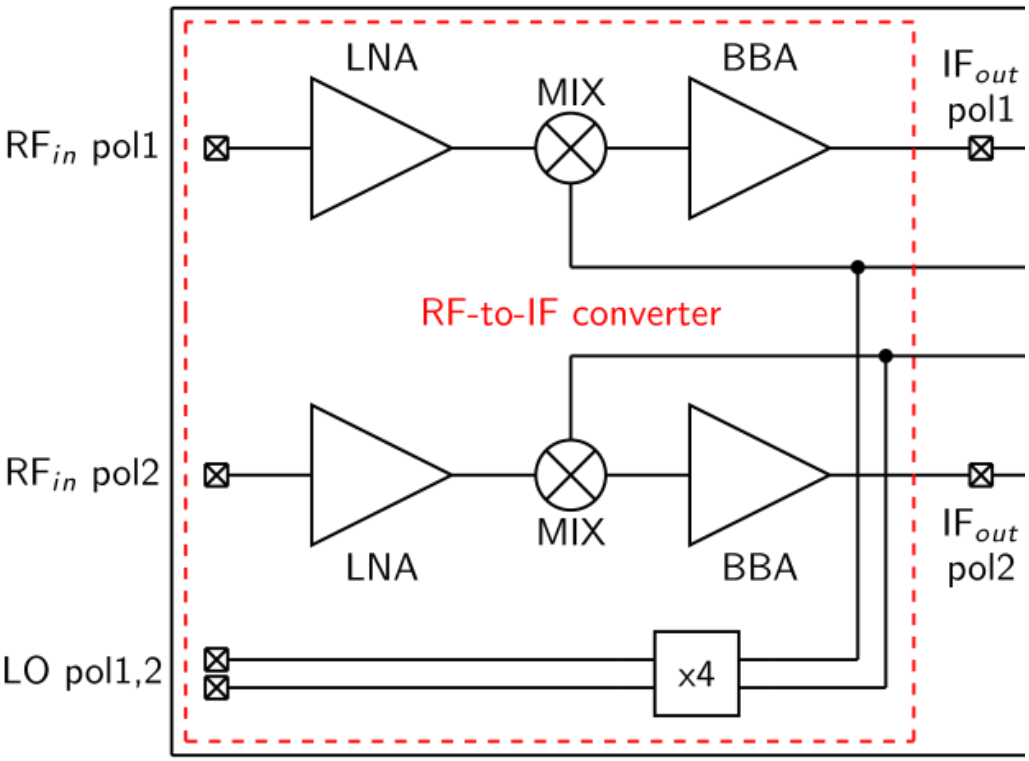
Receiver-Topology - RF-to-IF Converter

- Single-chip dual-channel receiver



Receiver-Topology - RF-to-IF Converter

- Single-chip dual-channel receiver



RF-receiver modules

- 28 nm CMOS
- Low-noise amplifier
- Down-conversion mixer
- Baseband amplifier (BBA)
- LO quadrupler 18 to 74 GHz

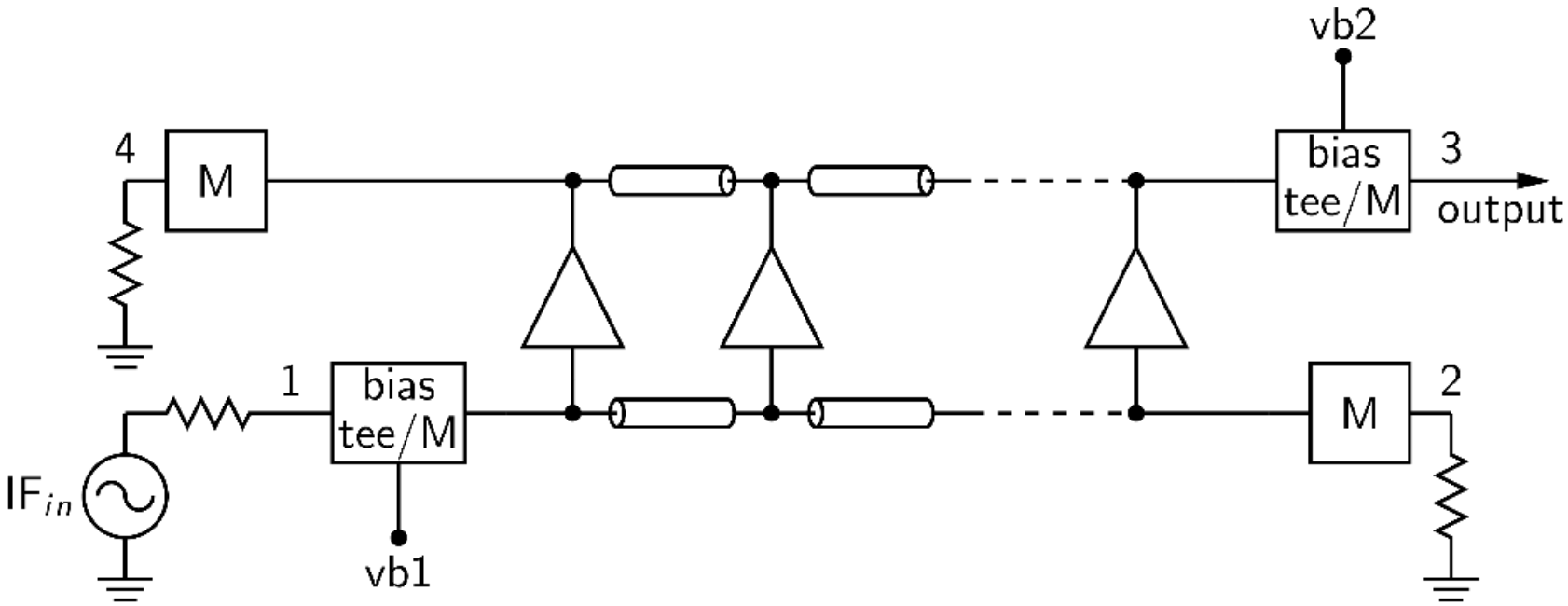
Features/Objectives

- Full W-band operation
- NF < 7 dB
- Analog gain > 55 dB
- BBA = 1 – 36 GHz (190% BW)
- Output power > 0 dBm

- Design challenge: baseband amplifier with 190 % bandwidth!

Baseband Amplifier 1 – 36 GHz

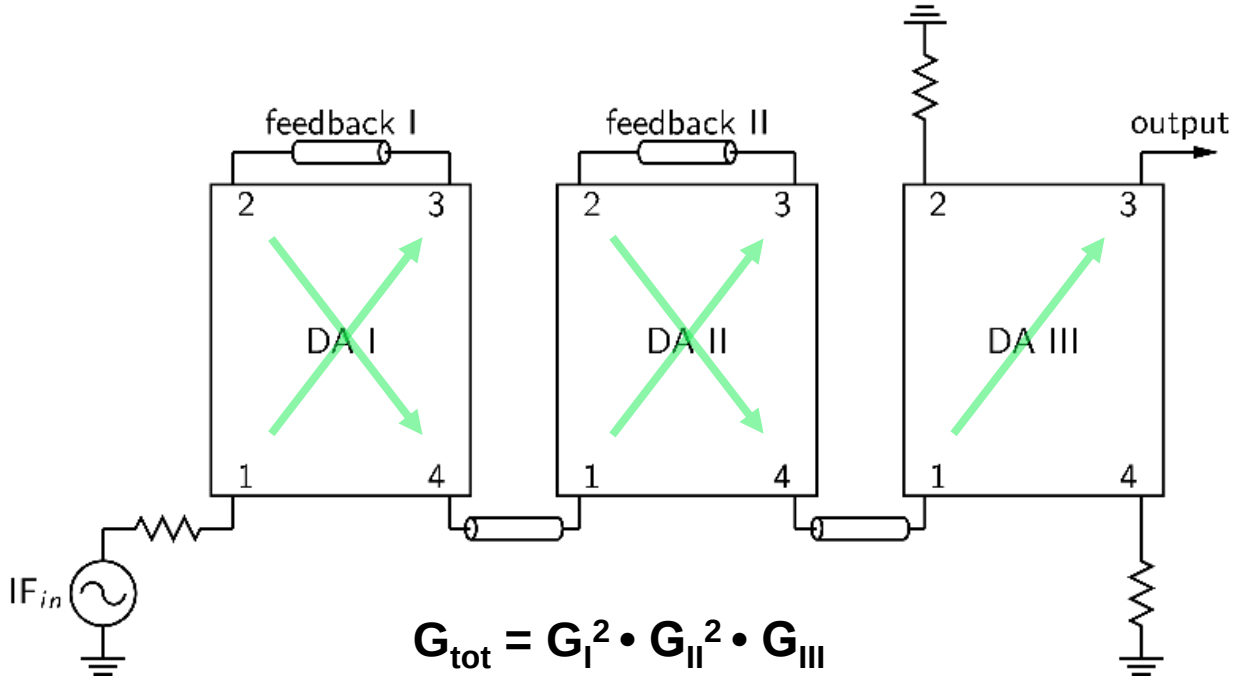
- How to achieve high gain with 190% relative bandwidth?



- Classic distributed amplifier (DA)
  - Pro: Inherently broadband
  - Con: low gain

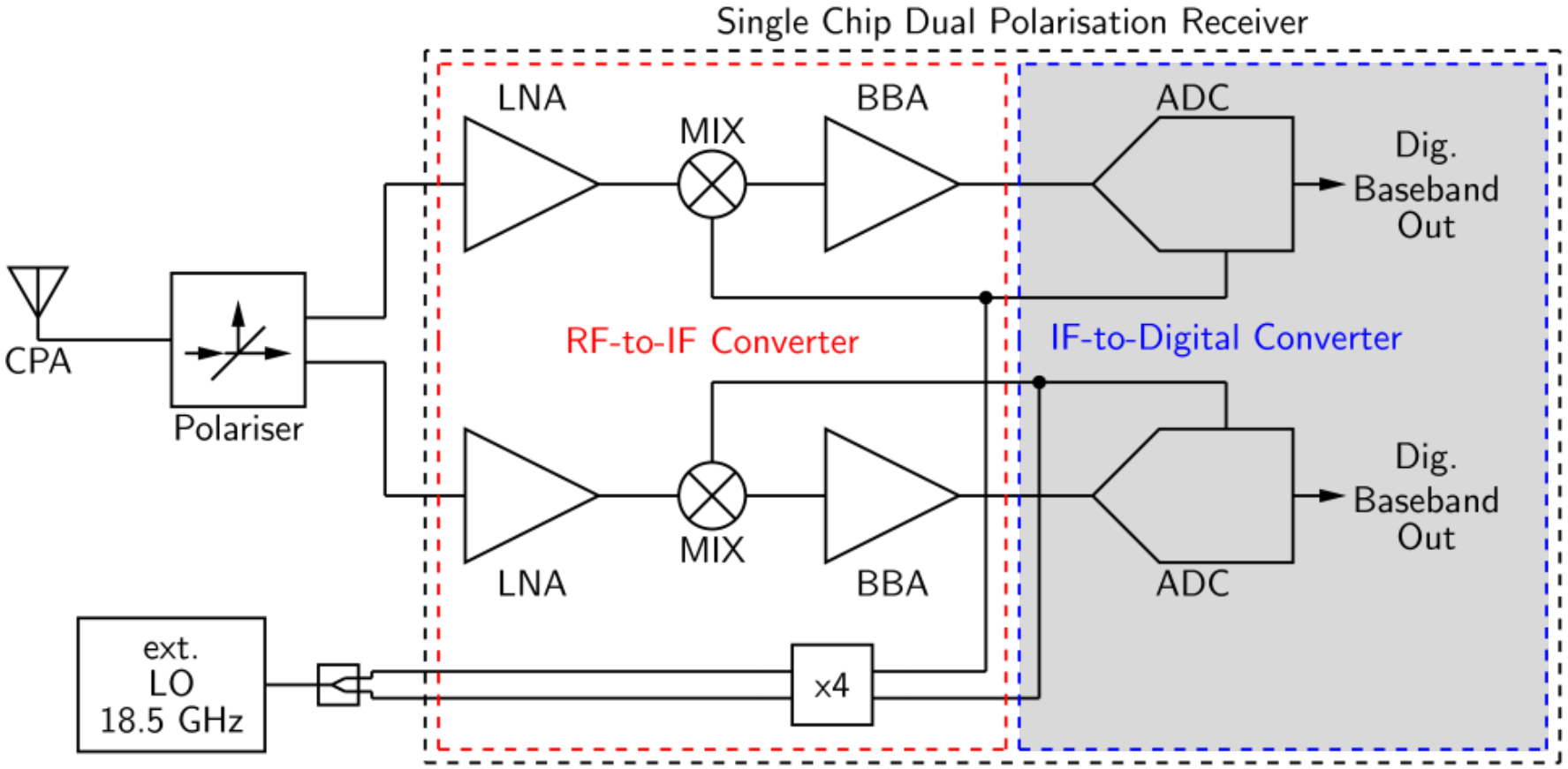
Baseband Amplifier 1 – 36 GHz

- How to achieve high gain with 190% relative bandwidth?



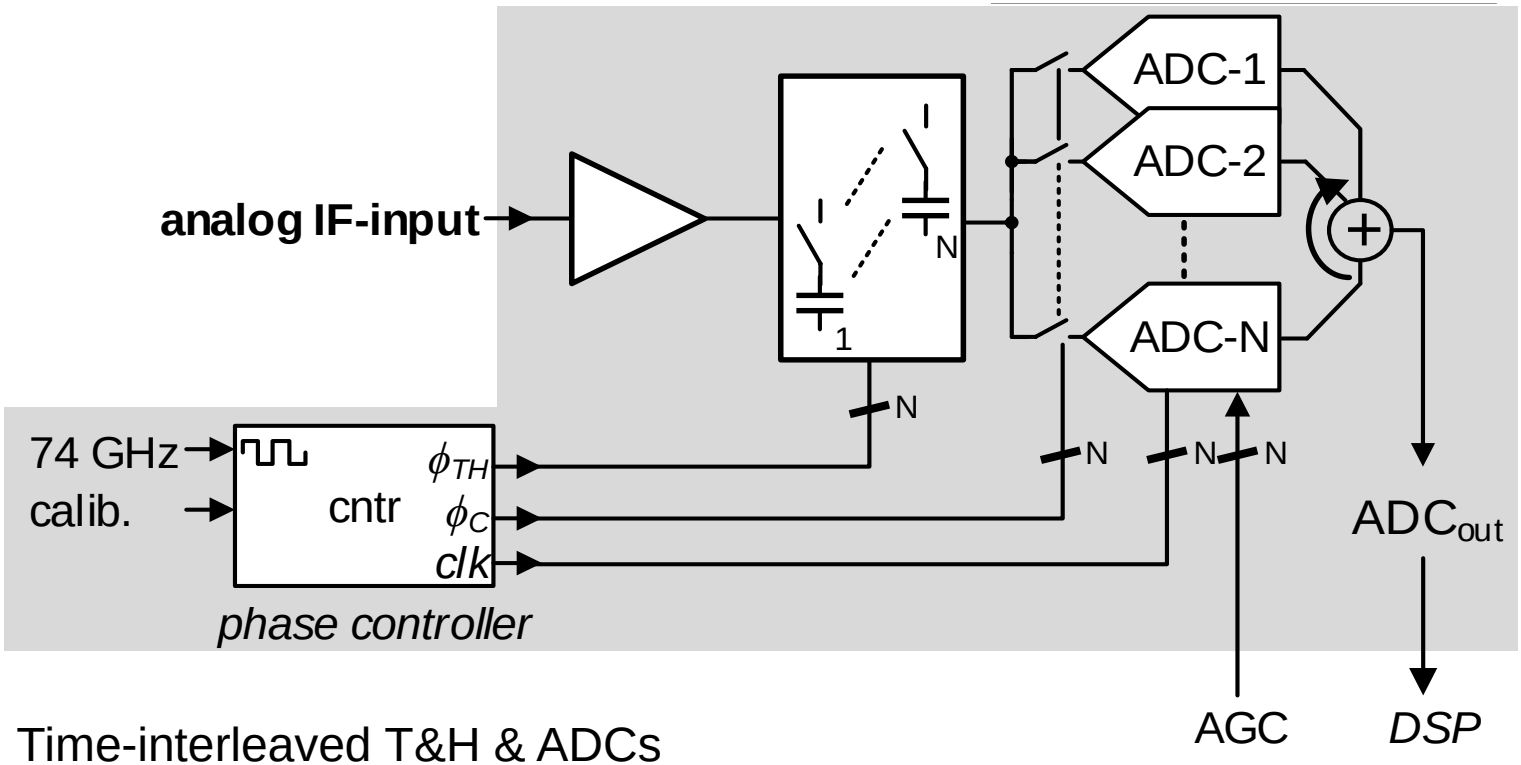
- Solution
  - Re-use forward and backward gain of DA
  - Multi-stage: combining 3 DA stages ➔ ~G^5

UWB IF-to-Digital Conversion – Overview



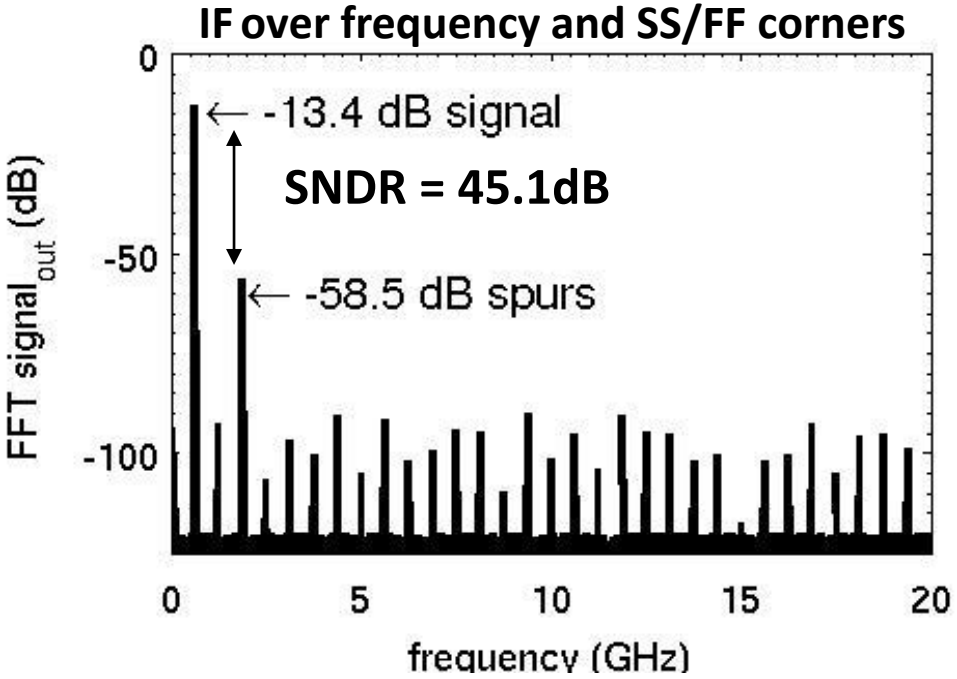
- Ultra-wideband (74GS/s) digitizer (direct UWB IF-to-digital conversion)
- >350Gbit/s effective RX resolution enabling simple modulation schemes (BPSK, QPSK) as well as channel equalization (offline)

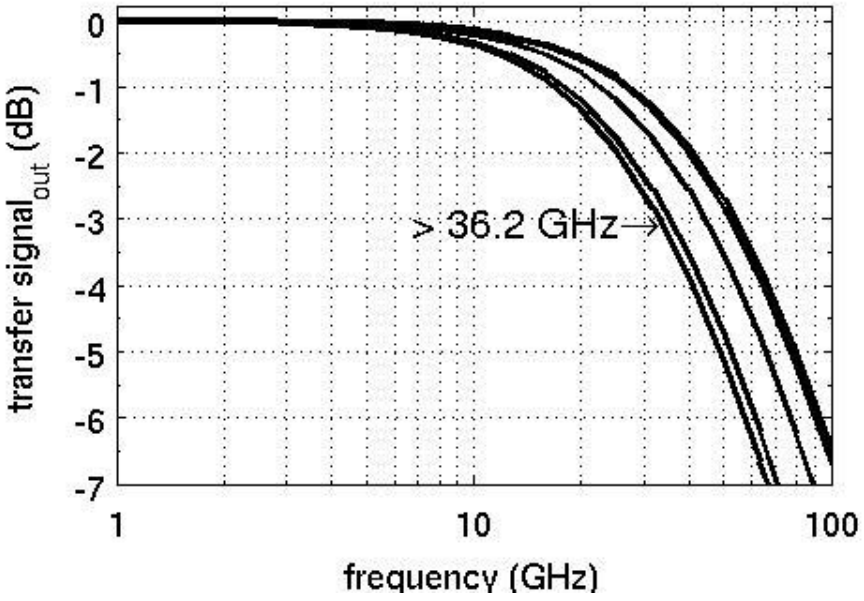
UWB IF-to-Digital Conversion – Overview



- Time-interleaved T&H & ADCs
- Impedance-conversion to drive T&H
- 40GHz T&H bandwidth with 6bit ENOB

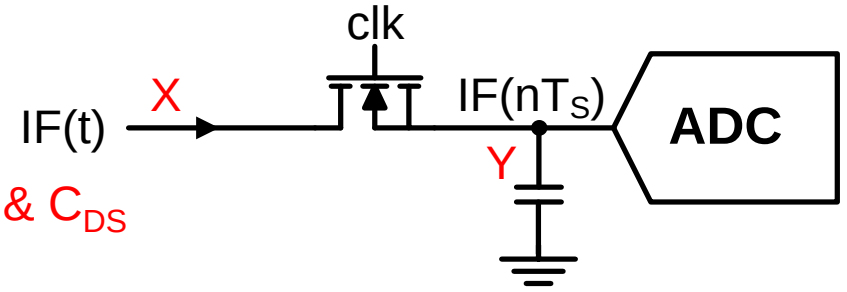
CMOS 28nm Technology Test





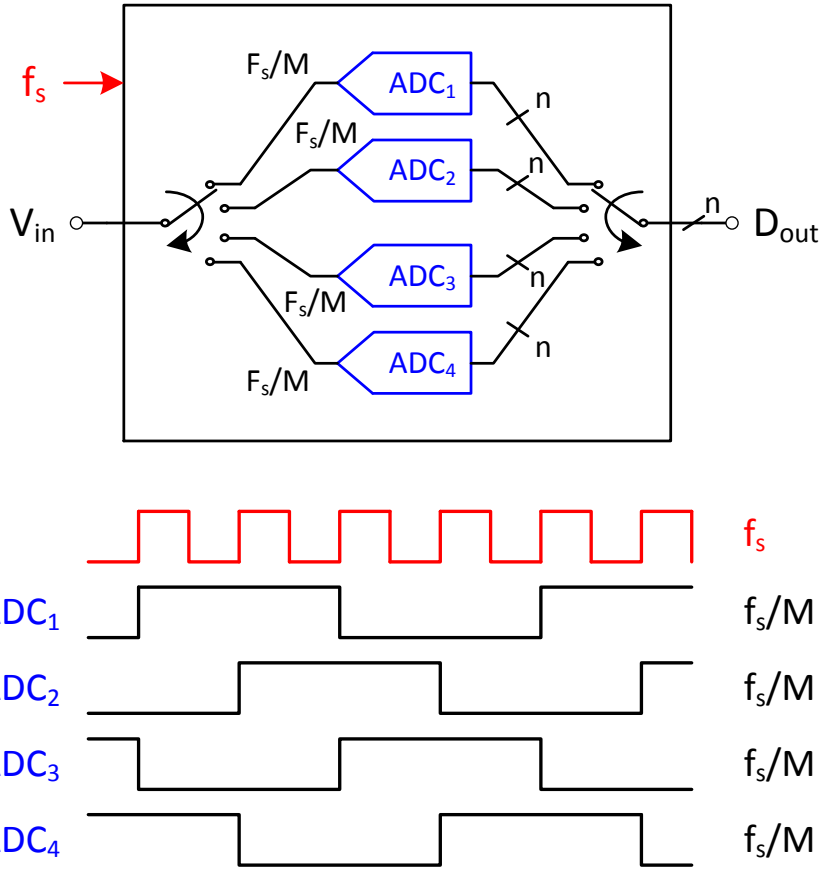
- R_{on} = 10-40 Ω
- $f_{T,n}$(TT) = 120 GHz
- C_{min} (kT/C) = 50 fF
- Challenge:
  switch performance limitation due to C_{GS} & C_{DS}

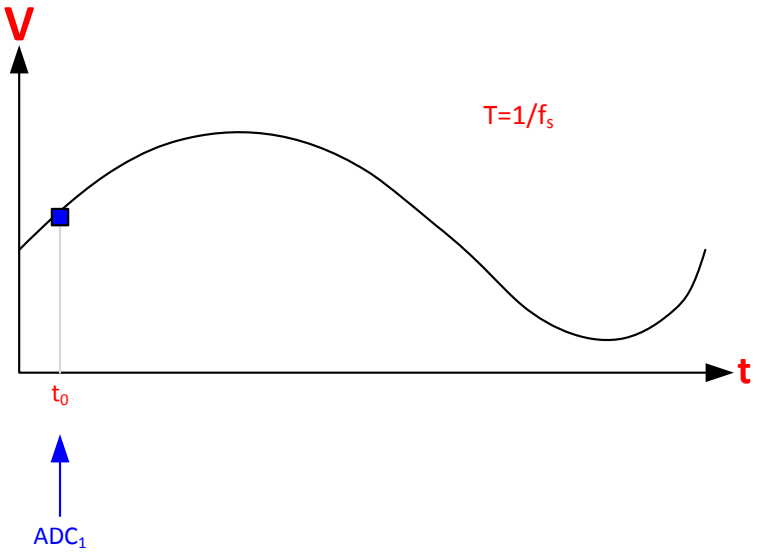
SNDR = 45.1 dB → 7.2 bit ENOB



Time-Interleaved ADC

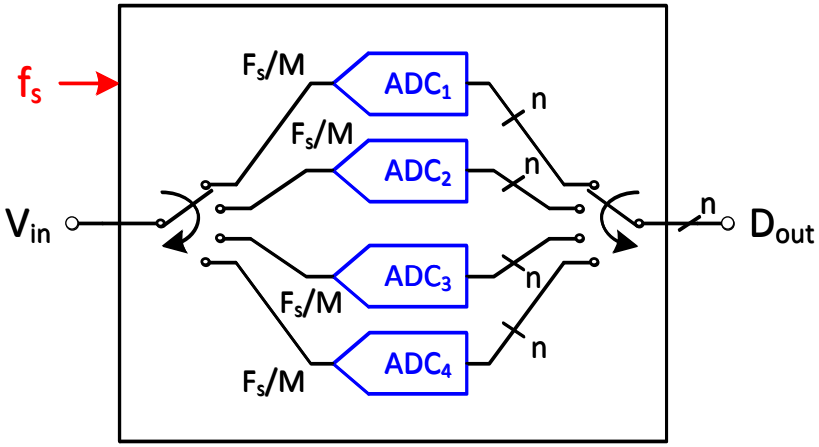
- Time-Interleaved ADC uses many parallel ADC channels operating at a lower speed (comparable with multiple CPU cores)

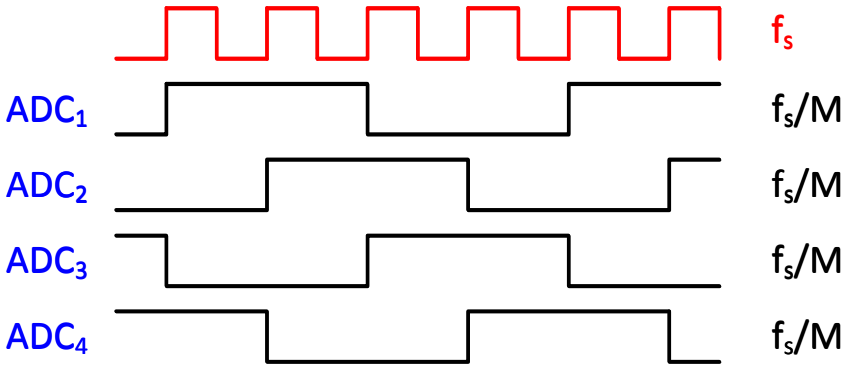


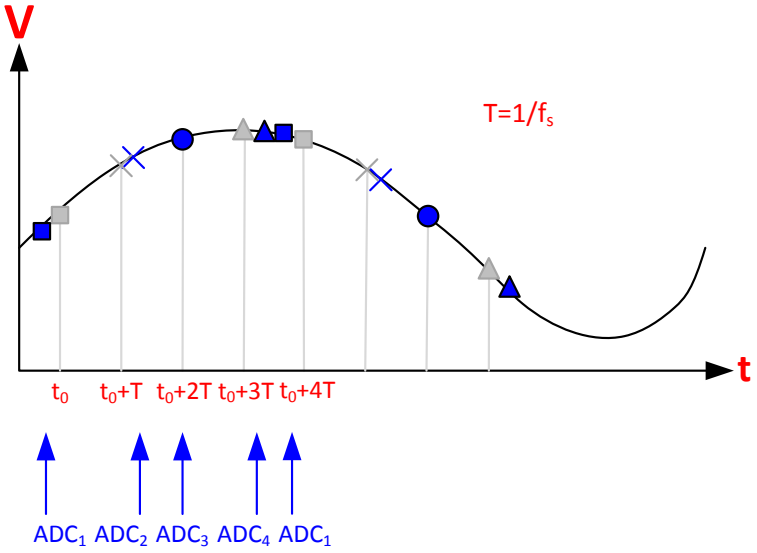


Time-Interleaved ADC

- Time-Interleaved ADC uses many parallel ADC channels operating at a lower speed (comparable with multiple CPU cores)







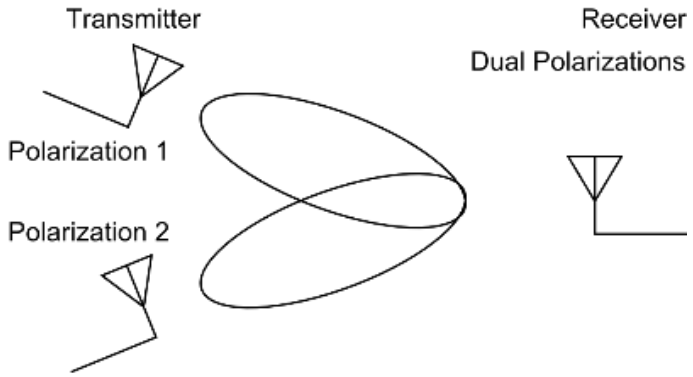
- Digital gain and offset mismatch calibration
- Mixed-signal timing mismatch calibration

100 Gb/s System Demonstrator

- CW system performance (TUHH anechoic chamber)

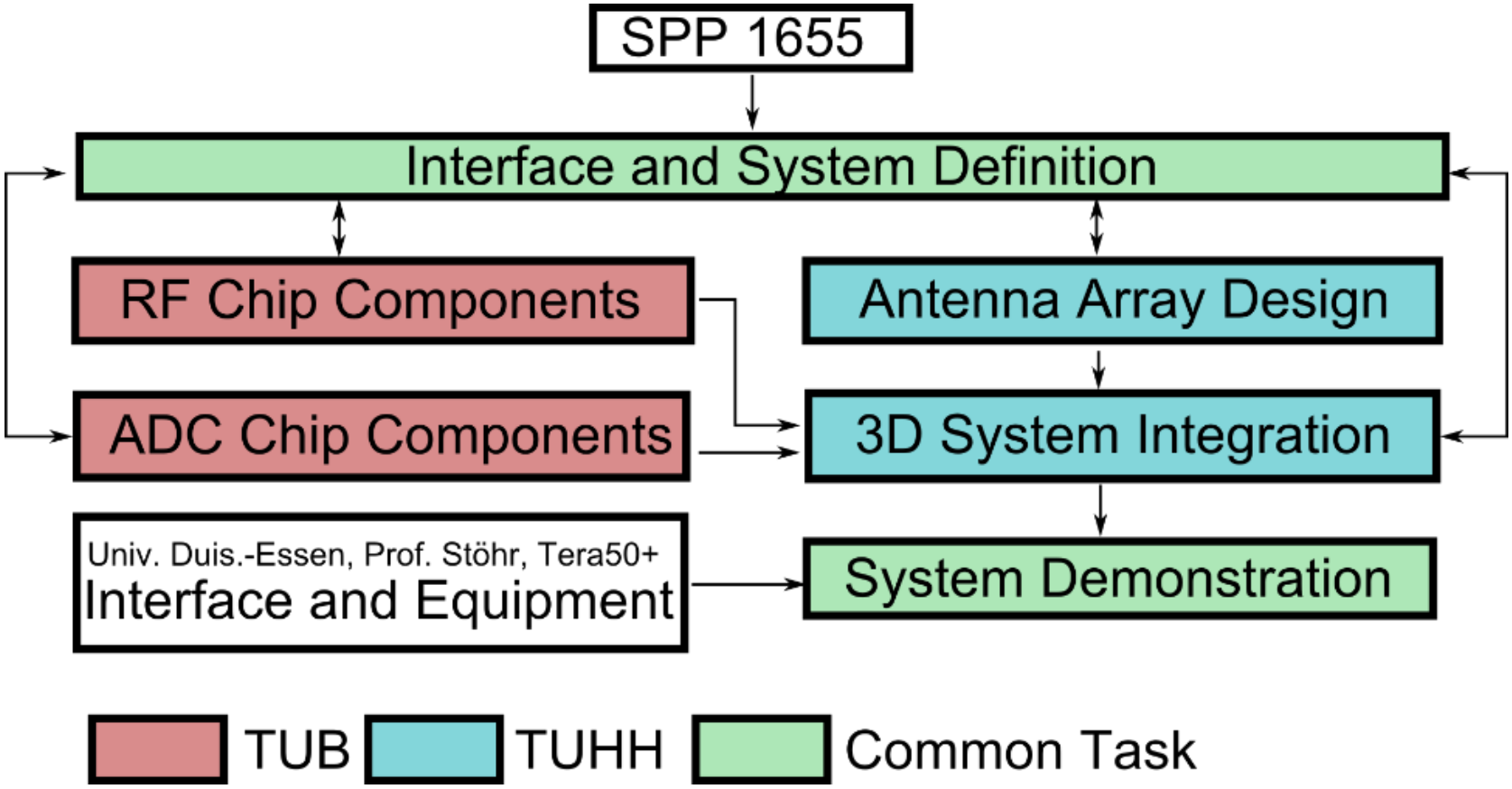
- Digital data communication
  - (Univ. Duisburg-Essen, SPP 1655/2 - Tera50+, Prof. Stöhr)

2 Options
- Analog IF outputs
- Digital outputs



System-level demonstration of 100 Gb/s W-band communication with digital beam steering

Collaboration Concept



Outline

1. Introduction
2. SPP 1655 – Project Results
3. SPP 1655/2 – Objectives
4. **Conclusions and Outlook**

Conclusions and Outlook

- **First project phase:** fully integrated low-cost transmitter with
  - CMOS BBPA and antenna array
  - dual circular polarization
  - system integration: work in progress

- **Second project phase:** fully integrated low-cost receiver with
  - single-chip receiver: LNA, BBA, down- and D/A-conversion
  - phased array with phase shifting LO
  - dual-polarization and independent steering
  - full-scale array and system demonstration

Thank you for your attention