Mixed-Mode Baseband for 100 Gbit/s Wireless Communication

J. Christoph Scheytt[1], Rolf Kraemer[2], Ingmar Kallfass[3]

[1]Heinz Nixdorf Institute, University of Paderborn, [2]BTU Cottbus-Senftenberg,
[3]University of Stuttgart

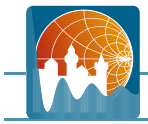
christoph.scheytt@hni.upb.de

Routes to 100 Gbps Wireless

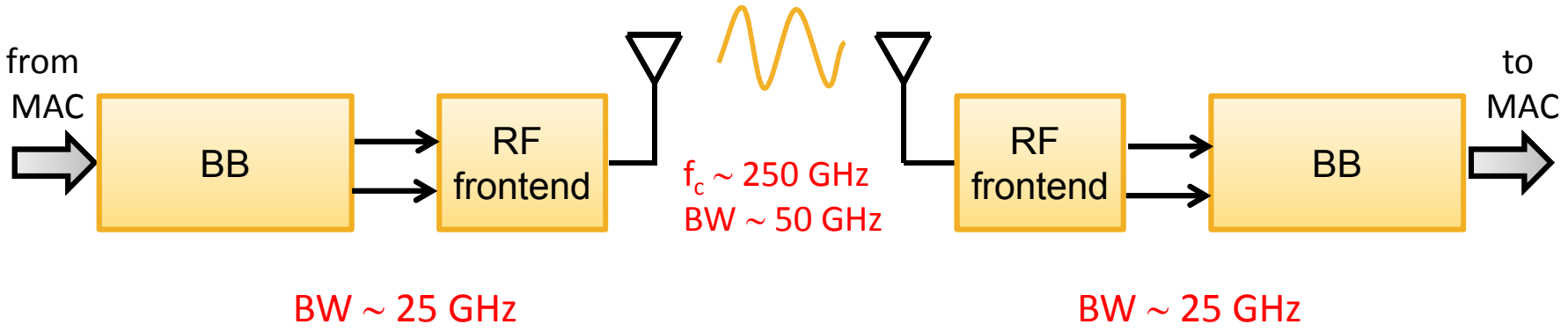
- Very high spectral efficiency with moderate bandwidth
  - 10 bit/sHz with 10 GHz BW
  - RF band e.g. V-band (60 GHz) or E-band (97-95 GHz)

- Moderate spectral efficiency with very large bandwidth
  - 2 – 4 bit/sHz with 25 – 50 GHz BW
  - RF mm-bands at 200 GHz or more

- Free space optics
  - e.g. 40 Gbaud with 8 PAM
  - 193 THz (λ=1550nm, infrared)
  - Potential for Tbit/s, using WDM



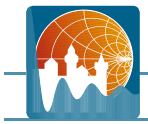
Wireless 100 Gb/s at f_c >200 GHz



- Our approach to 100 Gb/s Wireless focused on:
  - f_c > 200 GHz
  - Moderate spectral efficiency: 2 – 4 bit/sHz

→ High RF bandwidth (up to 50 GHz)

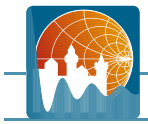
→ High baseband bandwidth (up to 25 GHz)



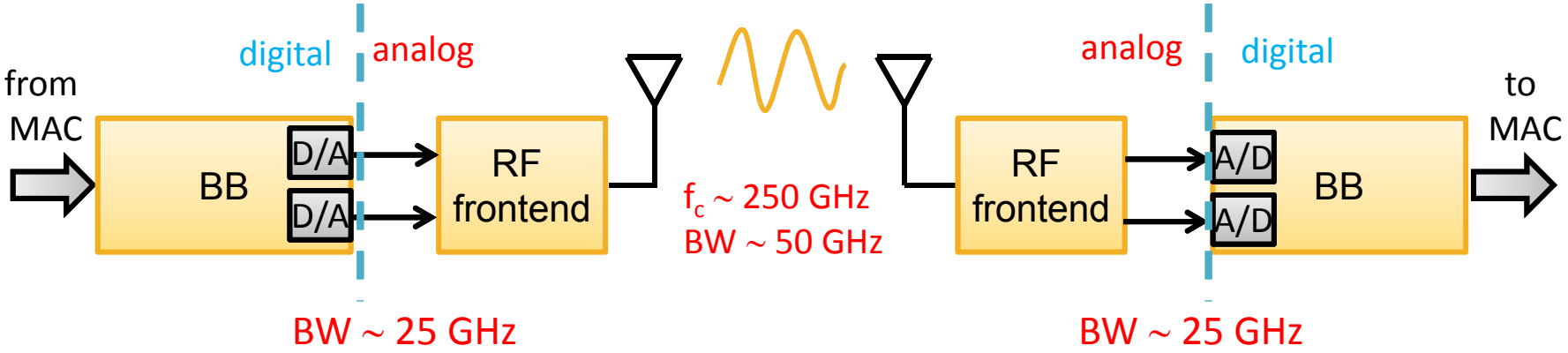
Wireless 100 Gb/s at f_c >200 GHz

data rate in Gbit/s	100	100	100	100	100
center frequency in GHz	61,5	275	275	275	275
modulation	2^20 QAM	4 PSK	4 PSK	4 PSK	4 PSK
number of channels	1	1	1	1	4
bandwidth per channel in GHz	5	50	50	50	12,5
SNR required for BER<10^-3 in dB	53,26	7,33	7,33	7,33	7,33
output power per channel in dBm	16	6	6	6	6
noise figure in dB	6	12	12	12	12
minimum required receive power in dBm	-17,58	-47,51	-47,51	-47,51	-53,53
Tx antenna gain in dBi	10	0	10	25	25
Rx antenna gain in dBi	10	0	10	25	5
margin / implementation loss in dB	10	10	10	10	10
maximum path loss in dB	43,58	43,51	63,51	93,51	79,53
achievable range in m	0,058598	0,012999	0,129994	4,110759	0,822152

- → Making assumptions on realistic BW, TX Power, RX NF etc. we will need highly directional antennas for range > 1m.

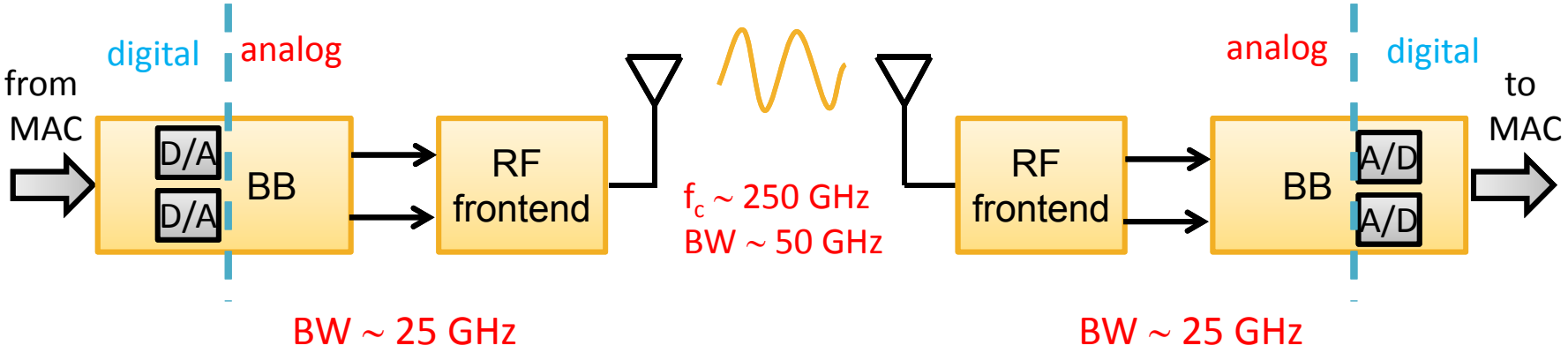


Challenges in 100 Gb/s Digital BB Approach



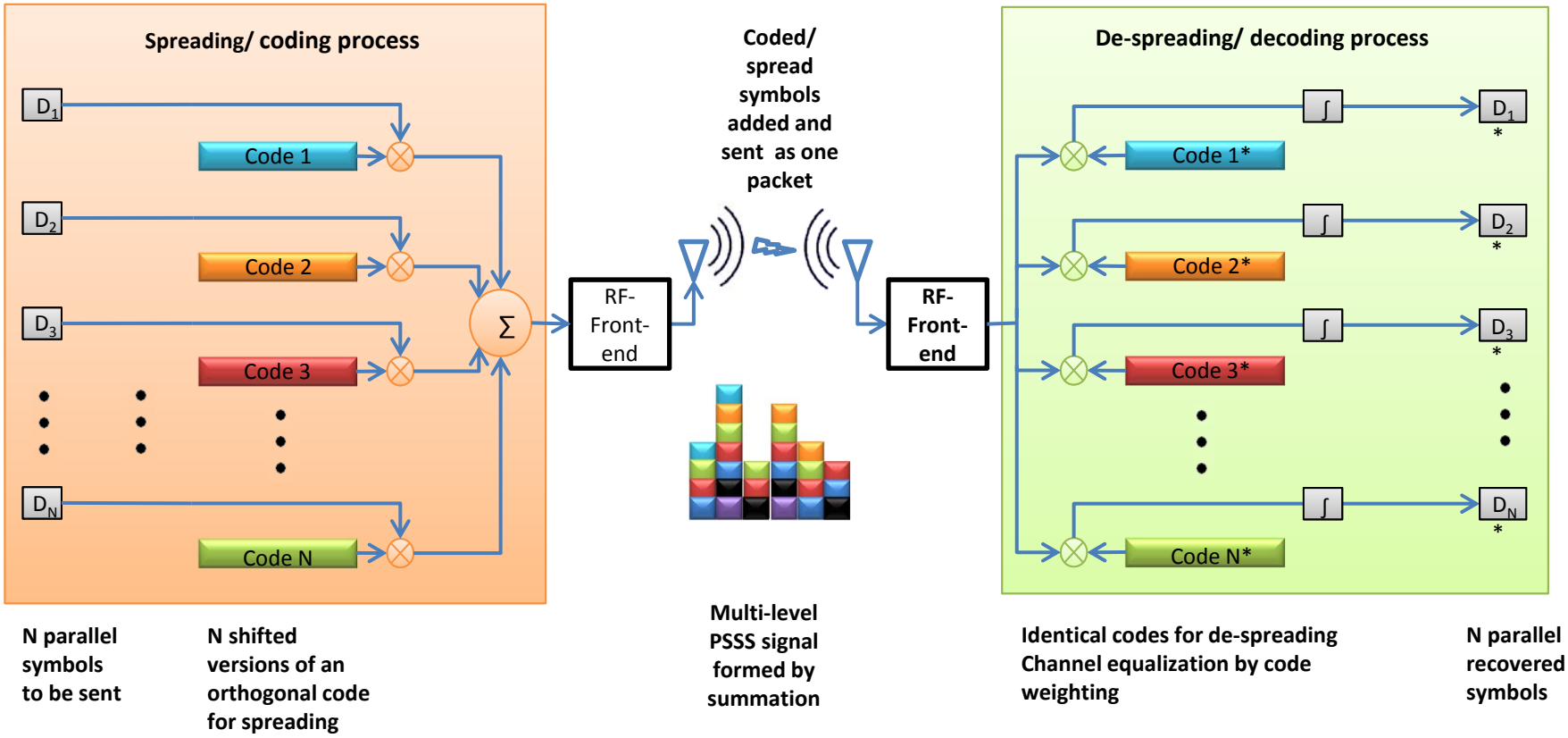
- Ultra-fast DACs/ADCs → power hungry, challenging design
- Many TFLOPs for signal processing → power hungry, complex hardware

100 Gb/s Mixed-Signal BB Approach



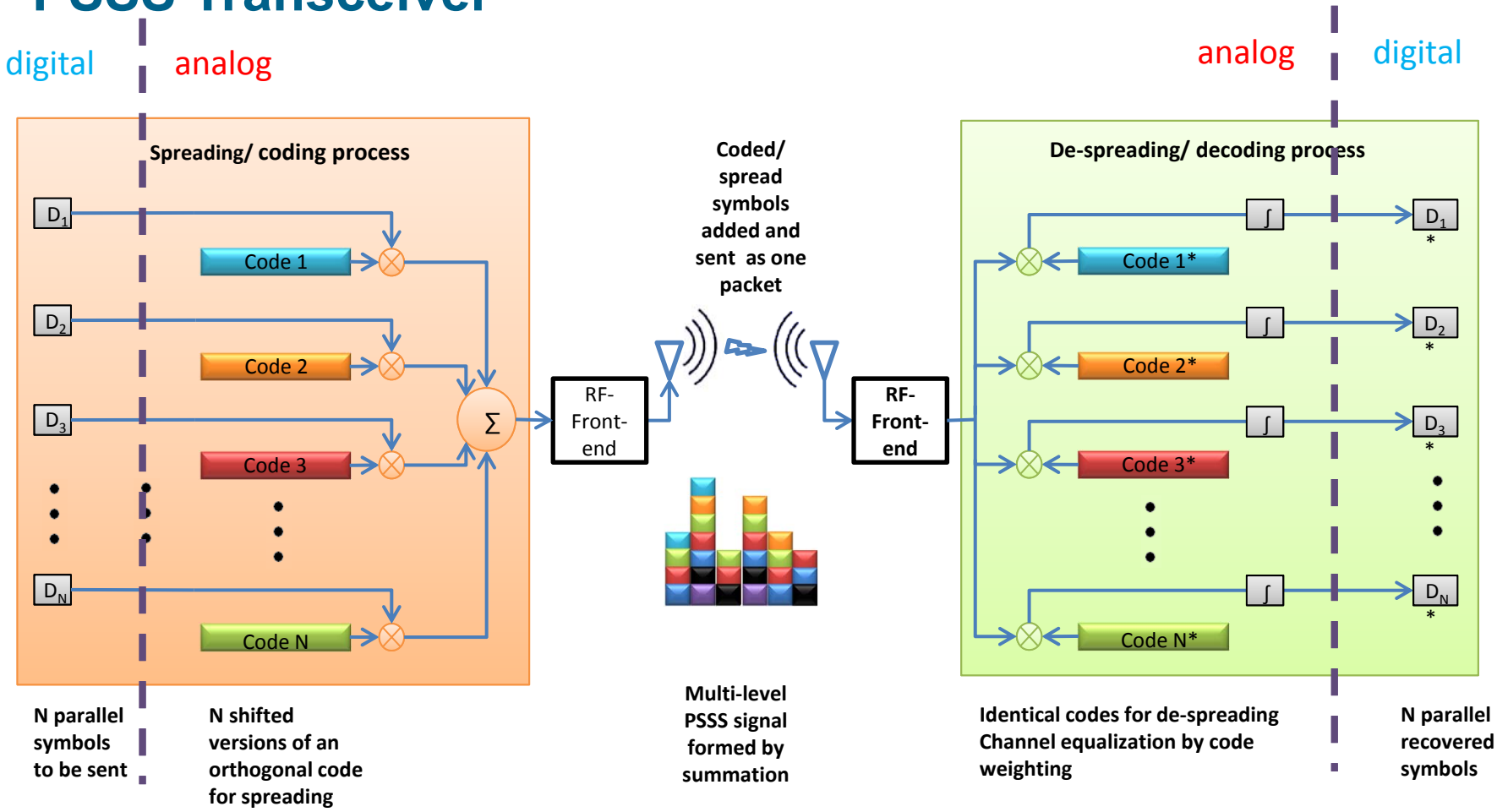
- Analog processing is inherently power and hardware-efficient, especially for broadband circuits.
- Shift analog/digital boundary → mixed-signal BB with significant analog processing
- „Analog-friendly“ modulation → Parallel Spread-Spectrum Seq. (PSSS)
- Efficient synchronisation → Coherent detection in analog/RF domain

PSSS Transceiver



- Parallel spread-spectrum sequencing (PSSS)
  = summation of DSSS streams (similar to HSPA)

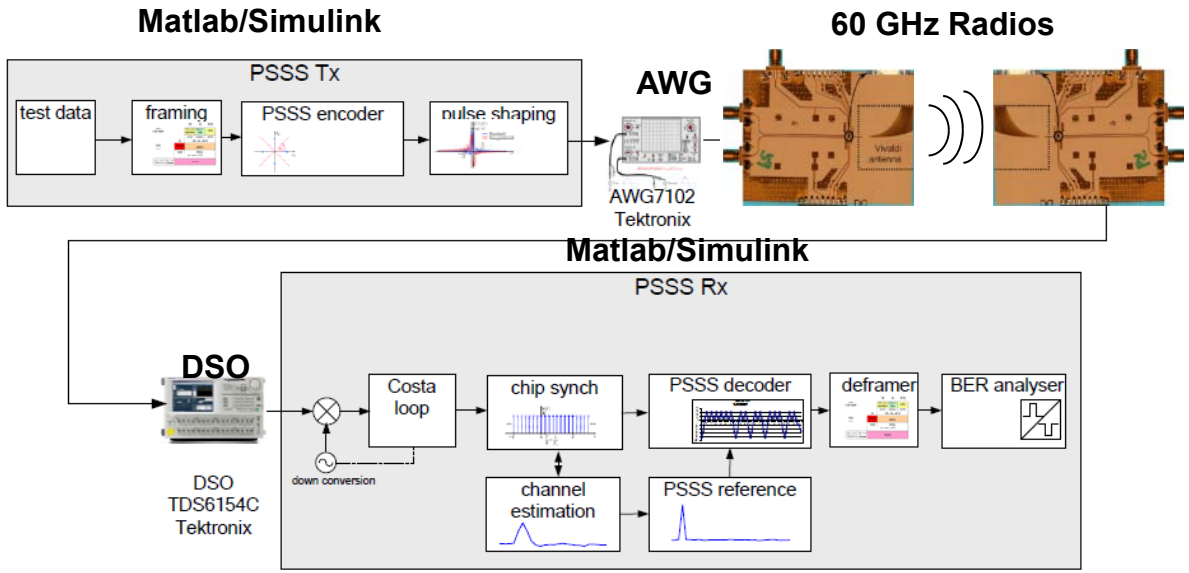
PSSS Transceiver



- Significant part of PSSS BB processing in analog/mixed-signal domain
  Low-speed DACs and ADCs operate at symbol rate.

PSSS System Design and Transmission Experiments

Using 60 GHz SiGe BiCMOS Transceivers

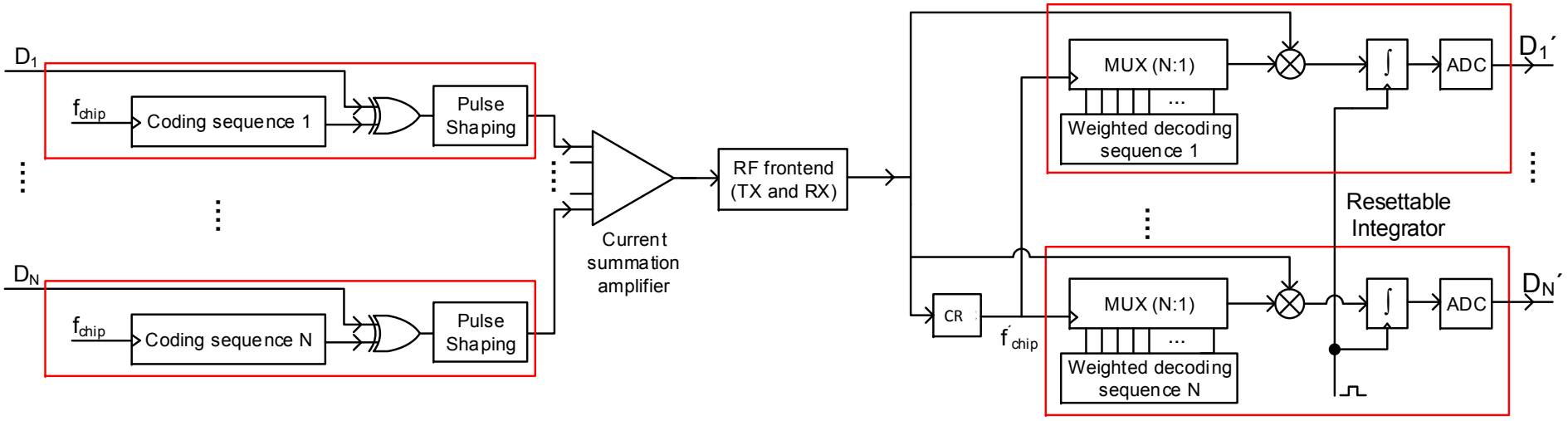


- Demonstration of PSSS[1] achieving 4 Gbps over 3m with BER of 1e−5
- Comparable to OFDM performance demo with same 60 GHz radios

[1] A. Wolf, R. Kraemer, J. C. Scheytt, "Ultra high speed wireless communication with low complexity transceiver," 2012 International Symposium on Signals, Systems, and Electronics (ISSSE)

Mixed-Signal PSSS BB Design

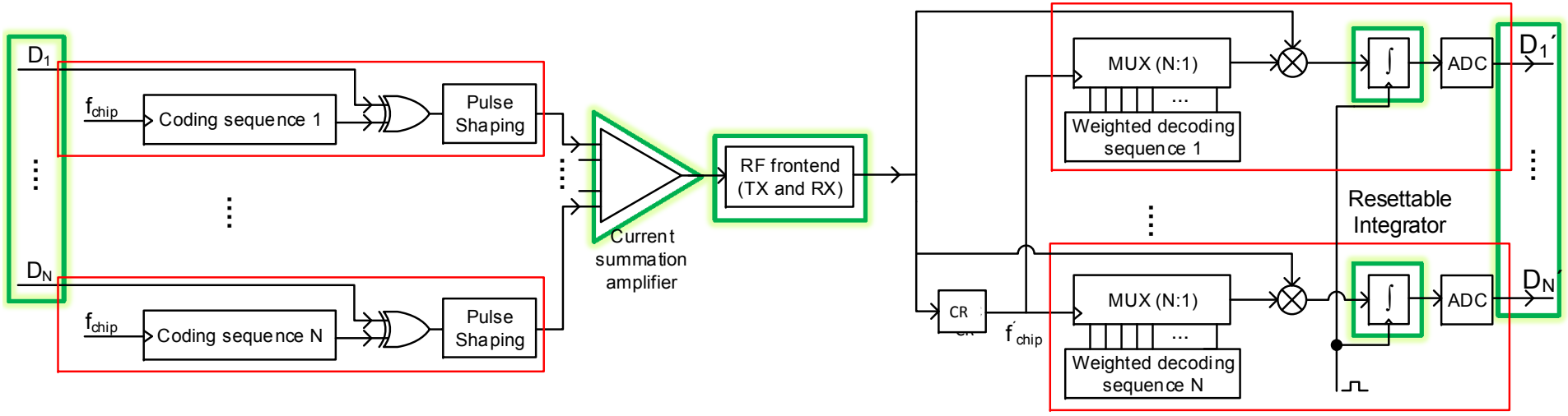
- N parallel symbols transmitted (TX)
- N parallel symbols recovered by means of cross correlation (RX)
- High speed data converters not required (TX, RX)
- Channel equalization by weighting the decoding sequence coefficients



Mixed-Signal PSSS BB Design

General Considerations

- Important factors for type and length of coding sequences:
- Input & output dynamic range of integrator (correlator) circuit
- Linearity & PAPR of the TX power amplifier
- Maximum no. of parallel symbols to be transmitted



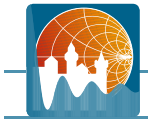
Mixed-Signal PSSS BB Design[1]

PSSS Coding Sequences

- Mixed signal PSSS baseband realization
  → chose shorter coding sequences
- Coding sequences considered:
  - Maximum length sequences (MLS or m-sequences): length 7, 15, or 31
  - Barker codes: length 7, 11, 13

MLS-15 turned out to be best choice for mixed signal PSSS BB implementation

[1] A. R. Javed, C. Scheytt: "System Design Considerations for a PSSS Transceiver for 100Gbps Wireless Communication with Emphasis on Mixed Signal Implementation ", IEEE WAMICOLN 2015



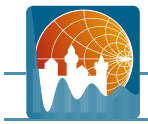
Mixed-Signal PSSS BB Design

PSSS Coding Sequences

- Unipolar $\{0,1\}$ and bipolar $\{-1,1\}$ variants of data vectors, coding sequences, and decoding sequences for MLS with code length N

	Data encoding			
	Unipolar		Bipolar	
	Coding sequences		Coding sequences	
	Unipolar	Bipolar	Unipolar	Bipolar
No. of PSSS levels (TX)	$\frac{N+3}{2}$	$N+1$	$\frac{N+3}{2}$	$N+1$
	Decoding sequences		Decoding sequences	
	Bipolar	Unipolar	Bipolar	Unipolar
Dynamic range at integrator input[1]	$\frac{N+1}{2}$	$\frac{N+1}{2}$	$\frac{N+1}{4}$	N

[1](max. input amplitude) / (min. input amplitude)



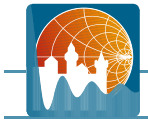
Mixed-Signal PSSS BB Design

PSSS Coding Sequences

- Comparison of MLS-15 with Barker-11 and Barker-13

	Data (bipolar)					
	Coding sequences (MLS-15)		Coding sequences (Barker-11)		Coding sequences (Barker-13)	
	Unipolar	Bipolar	Unipolar	Bipolar	Unipolar	Bipolar
No. of PSSS levels	9	16	6	12	10	14
	Decoding sequences		Decoding sequences		Decoding sequences	
	Bipolar	Unipolar	Bipolar+ 0.2*	Unipolar- 1.0*	Bipolar- 0.33*	Unipolar- 0.6*
Dynamic range at integrator input	4	15	6	11	12	8

* For barker codes a DC offset is required in the decoding sequence

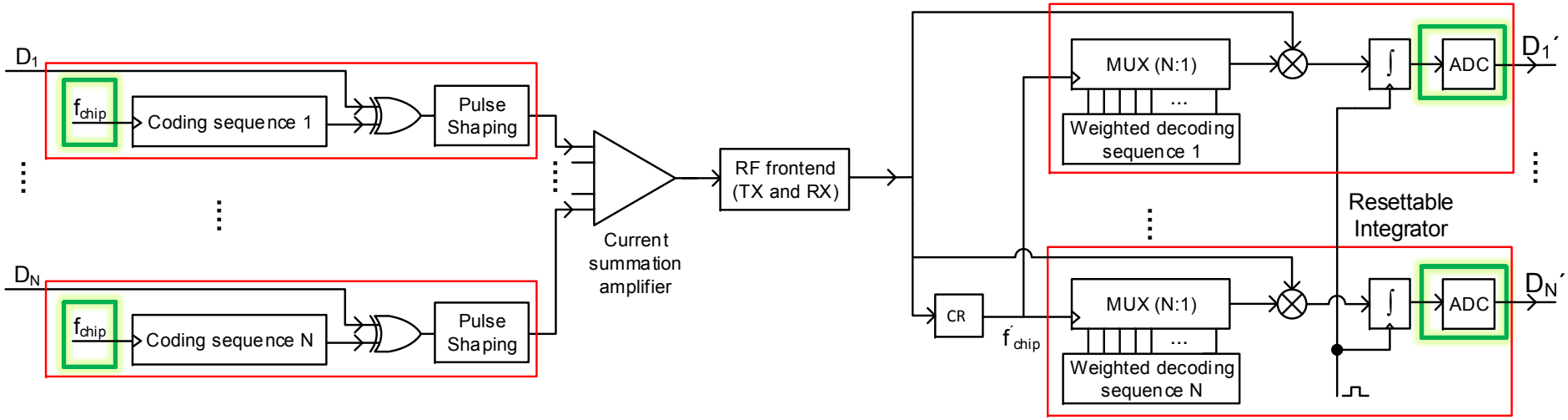


Mixed-Signal PSSS BB Design

Chip Rate

- Maximum realizable chip rate: 25–30 Gcps (0.13µm BiCMOS)
- Minimum bit loading required: $4\ \frac{bit}{symbol}$ since

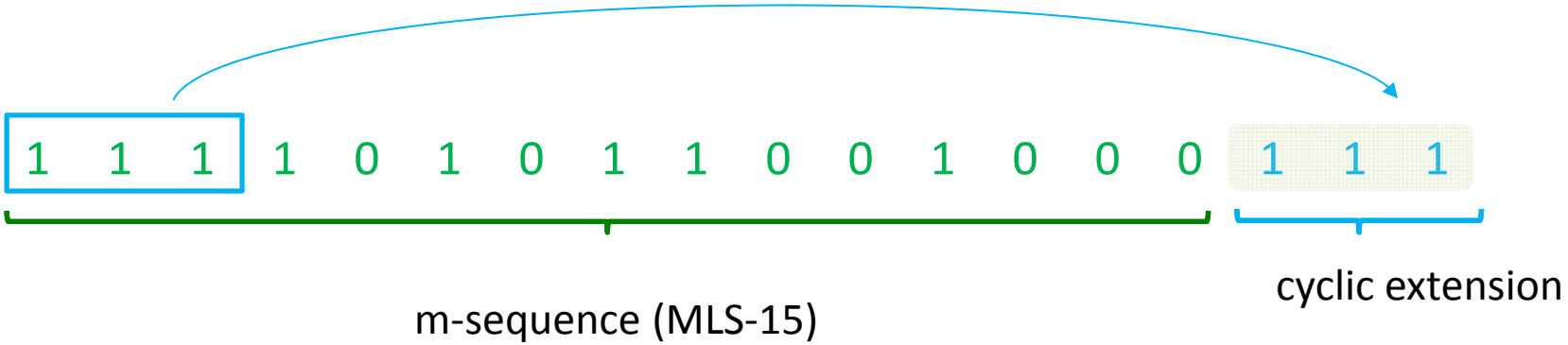
$$25\frac{Gsymbols}{sec} \times 4\ \frac{bit}{symbol} = 100\ \frac{Gbit}{\text{sec}}$$



Mixed-Signal PSSS BB Design

Cyclic Extension

- Guard interval (cyclic extension) added to avoid ISI between PSSS blocks.
- Mixed signal implementation => fixed length of cyclic extension.
- Assuming a dircect line of sight link with highly directive antennas, an estimated value of $3\ T_{chip}$ is assumed.



Mixed-Signal PSSS BB Design

Cyclic Extension

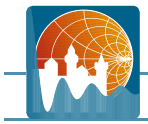
- Cyclic extension reduces link utility

$$Link\ utility = \frac{Time\ for\ payload\ data}{Total\ time\ for\ data\ transaction} = \frac{15}{15+3} = 83.33\%$$

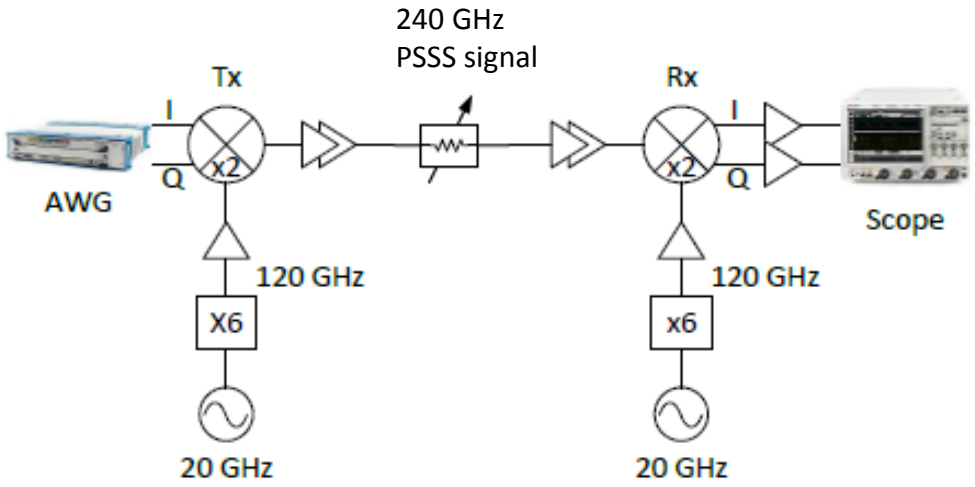
- Chip rate can be increased to restore net data rate to 100 Gbps i.e.

$$25Gcps \times \frac{1}{0.8333} = 30Gcps$$

- Cyclic extension: $3\ T_{chip} = 3 \times \frac{1}{30\ Gcps} = 100\ ps$

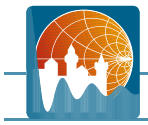


PSSS Hardware-in-the-loop Experiment @ 240 GHz

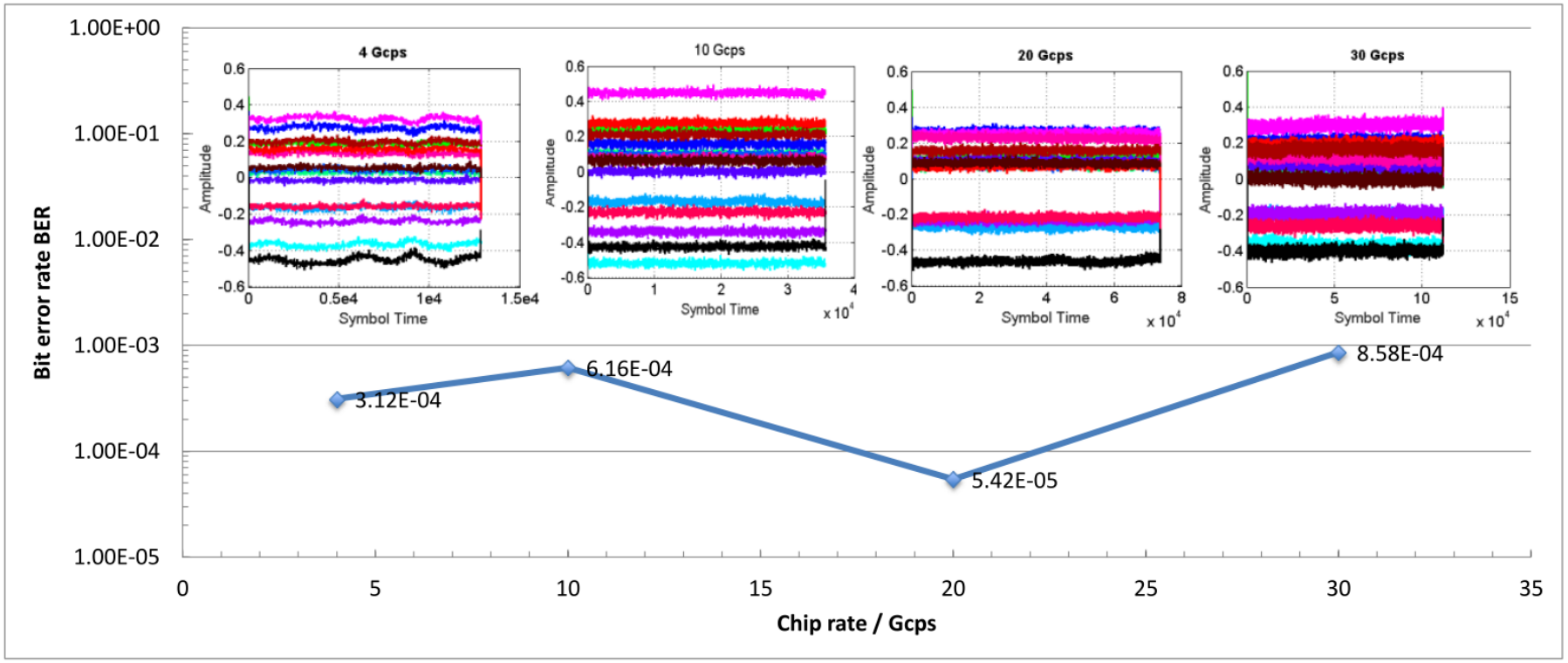


Parameter	Value	Description
N	15	# of PSSS streams
Coding sequence	MLS-15	15 bit MLS cyclic-shifted
Modulation	PAM-2	1 bits/symbol
F_{chip}	30 Gchip/s	Chip rate
N_{guard}	3	Guard interval (# of chips)
f_{symbol}	1.67 GSym/s	Symbol rate

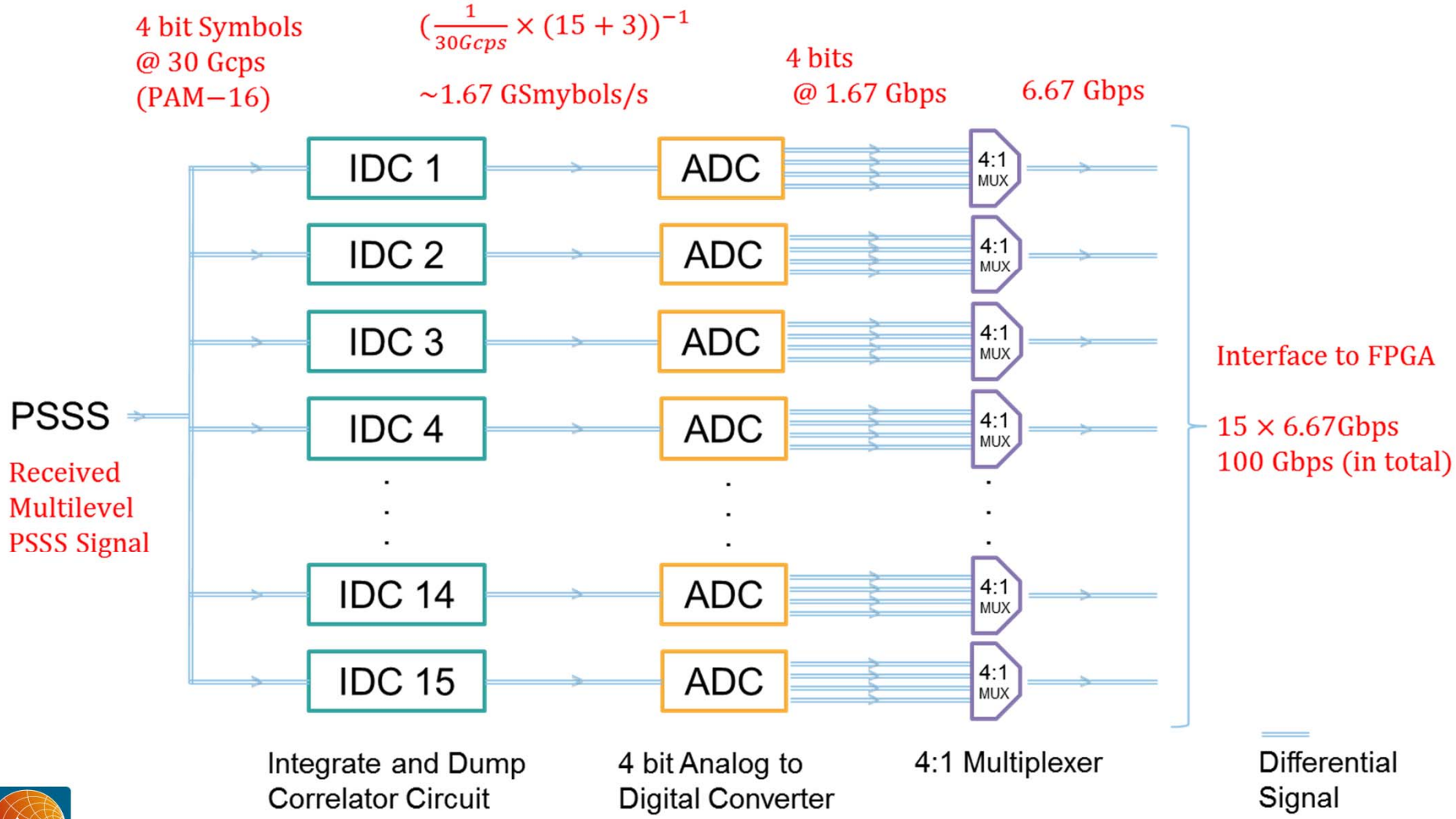
- PSSS baseband signals loaded to AWG
- 240 GHz GaAs RF transmitter and receiver
- Antennas replaced by attenuator
- DSO data processed with Matlab PSSS receiver model
- Only 2-level modulation limited RF frontend linearity



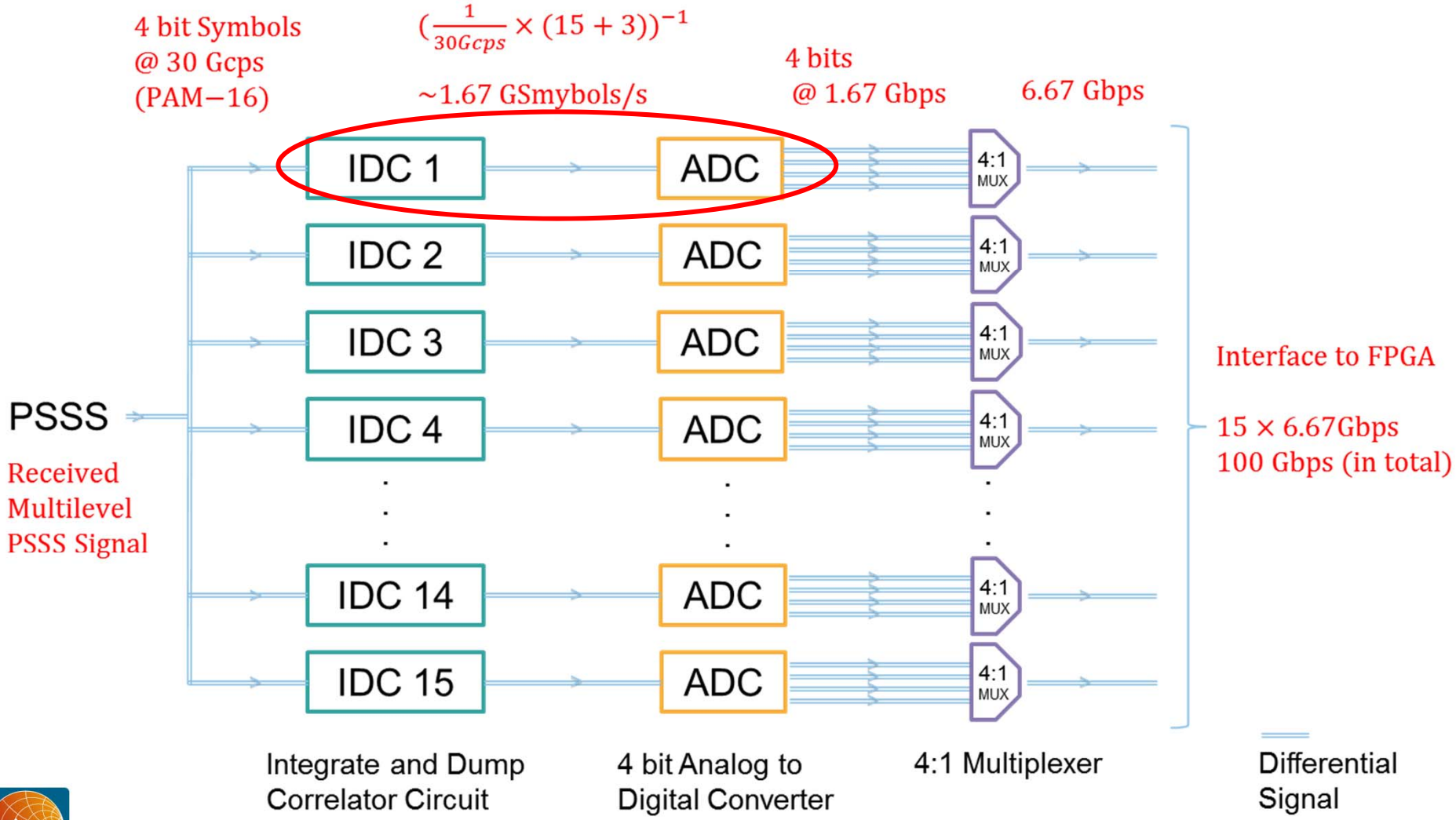
PSSS Hardware-in-the-loop Experiment @ 240 GHz



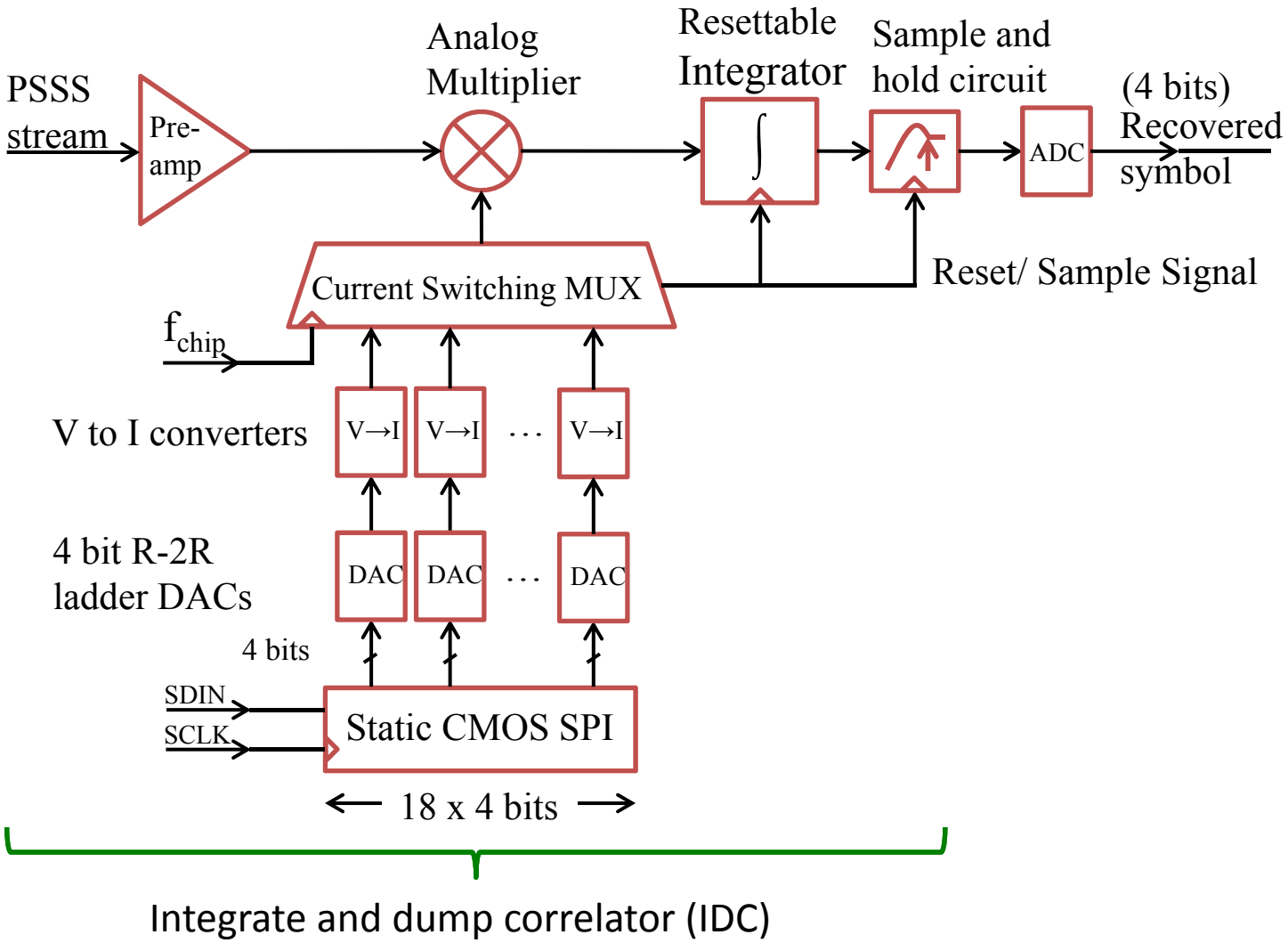
PSSS Mixed-Signal Receiver Block Diagram



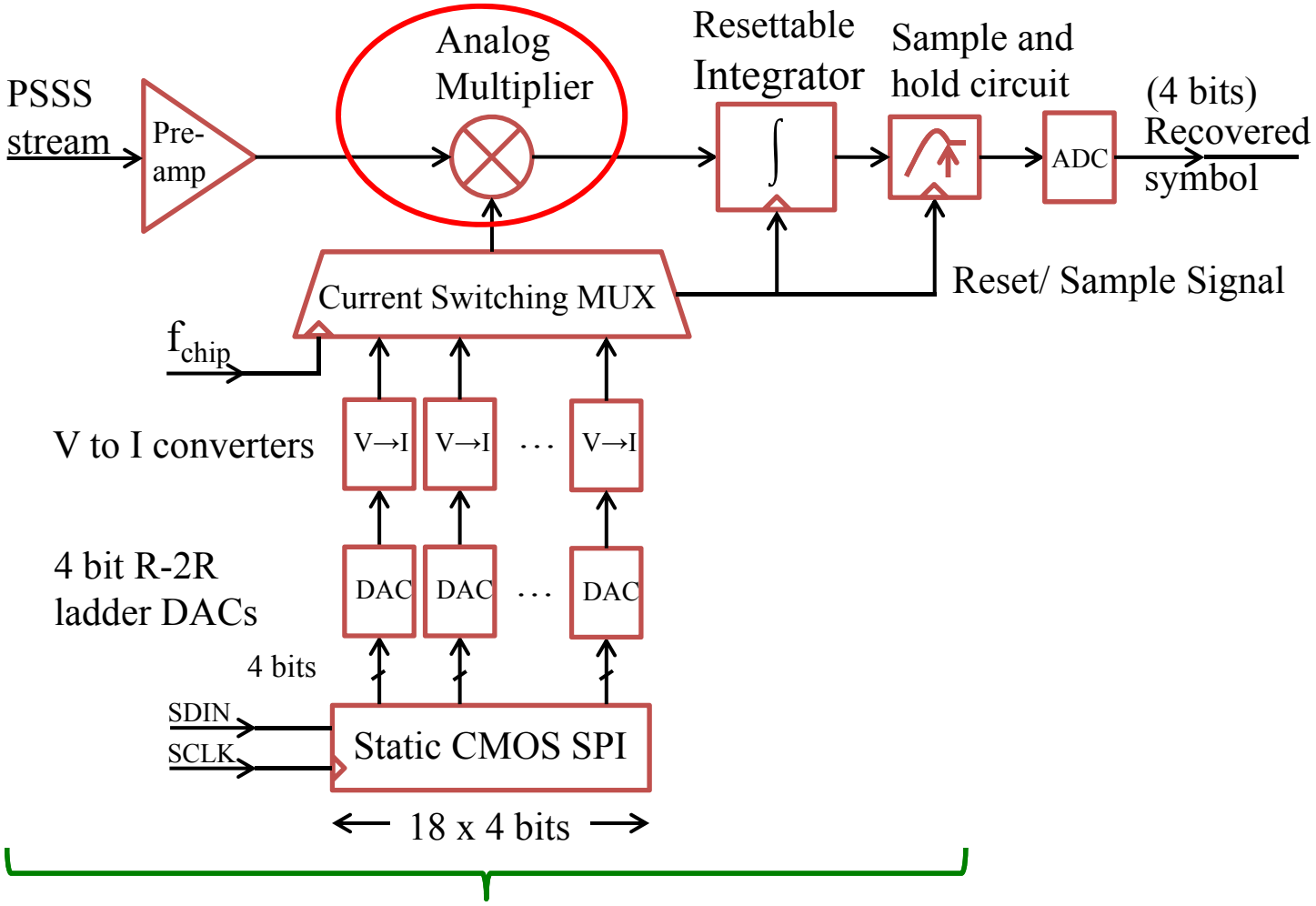
PSSS Mixed-Signal Receiver Block Diagram



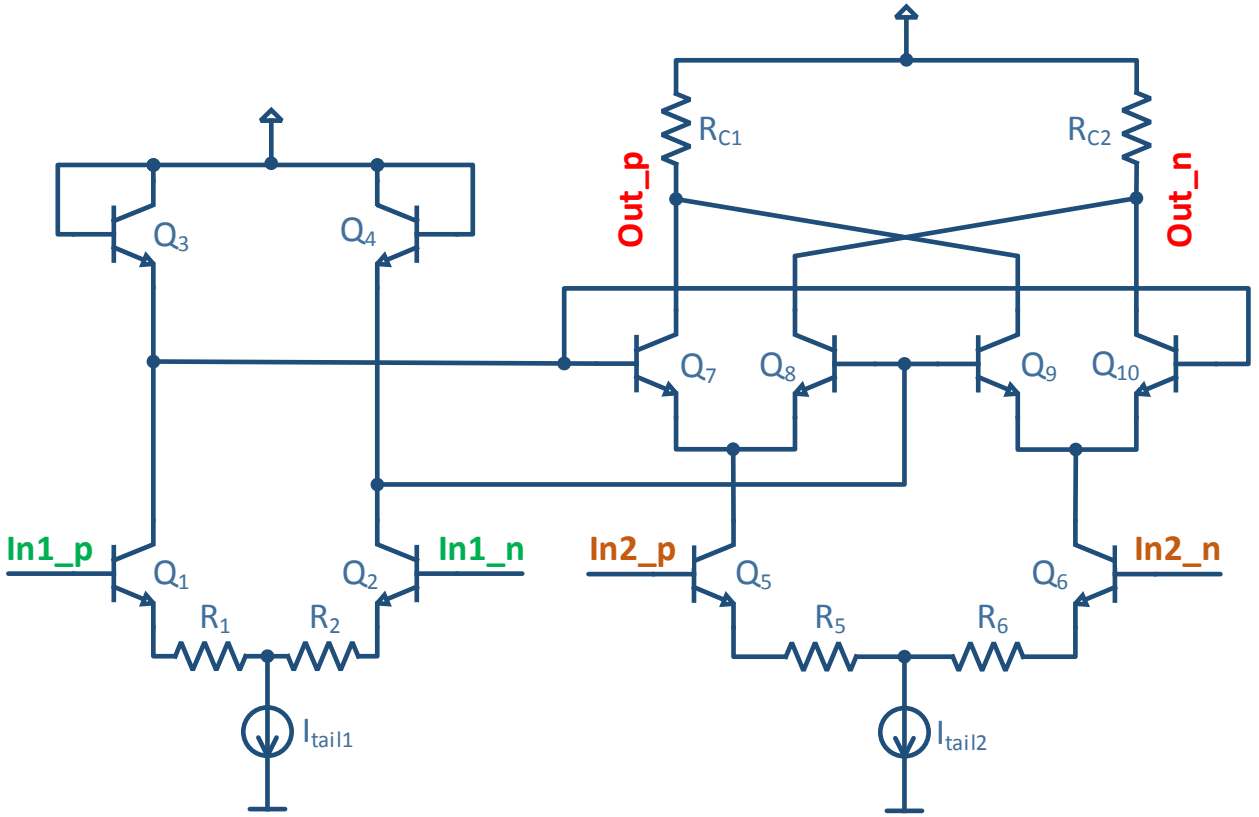
Integrate and Dump Correlator Circuit w. ADC



Integrate and Dump Correlator Circuit w. ADC

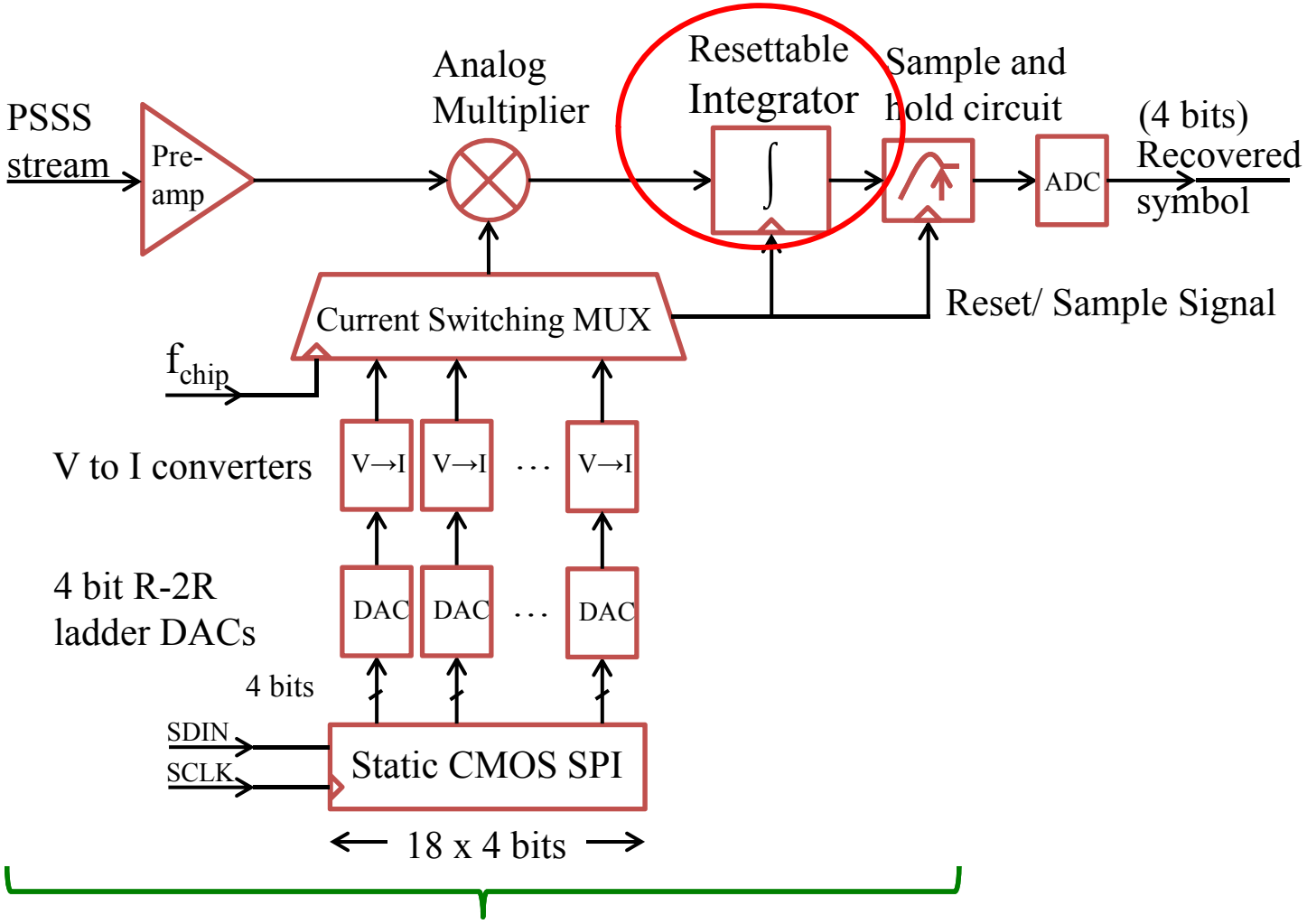


Analog 4-Quadrant Multiplier

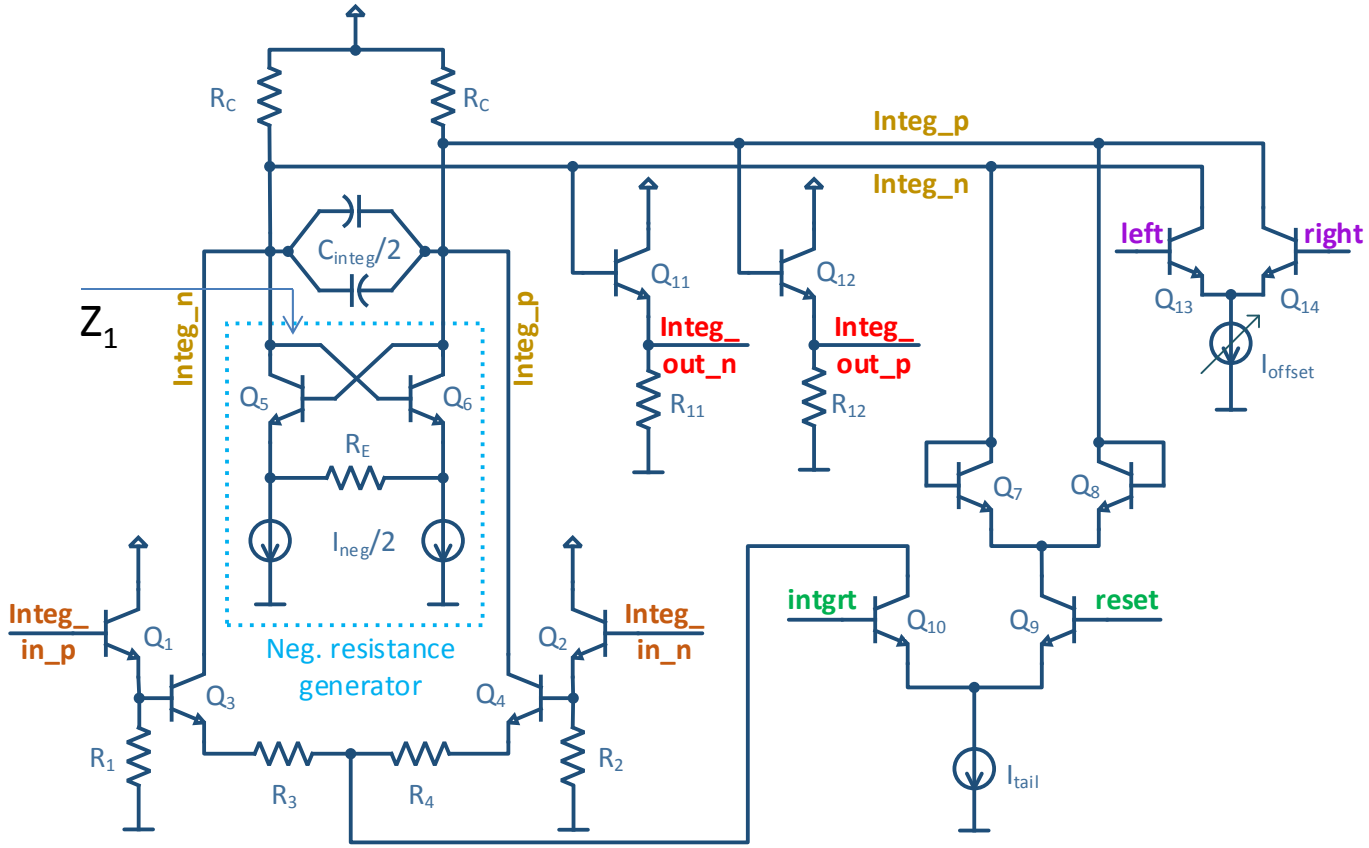


- Gilbert Cell operated as linear broadband analog multiplier

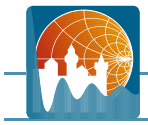
Integrate and Dump Correlator Circuit w. ADC



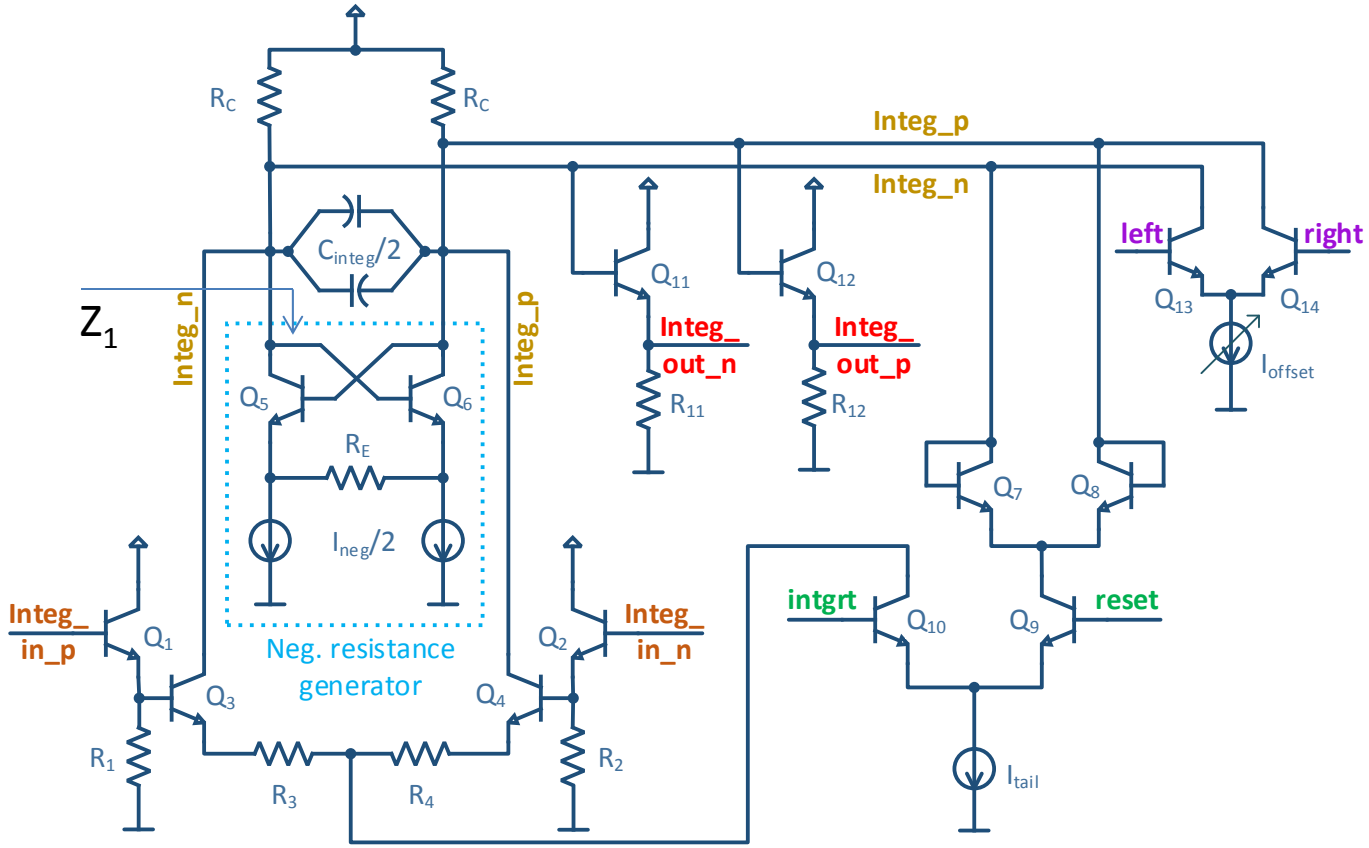
Broadband Resettable Integrator



- Q_5, Q_6 and R_E operate as negative resistance generator w. $Z_1 = -2R_C$
- Hence R_C is cancelled and output currents of Q3 and Q4 is integrated by C_{integ}. –> extreme broadband integrator.



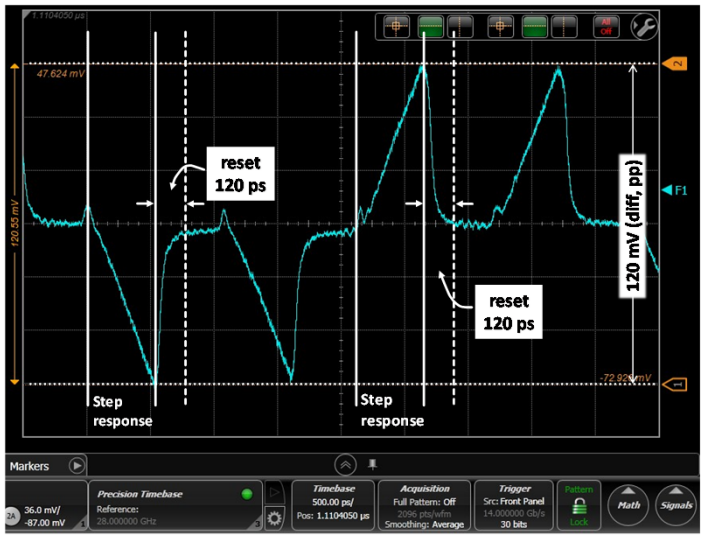
Broadband Resettable Integrator

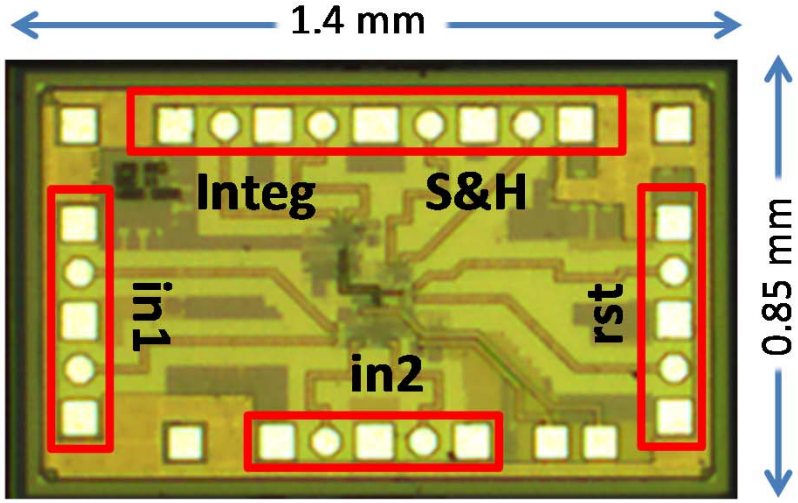


- Q_3, R_3 Q_4, R_4 represent linear V-I converters
- Q_9, Q_{10} control integrate and reset phase

Q_{13}, Q_{14} , I_{offset} implement integrator offset control

Broadband Resettable Correlator Test Chip[1]

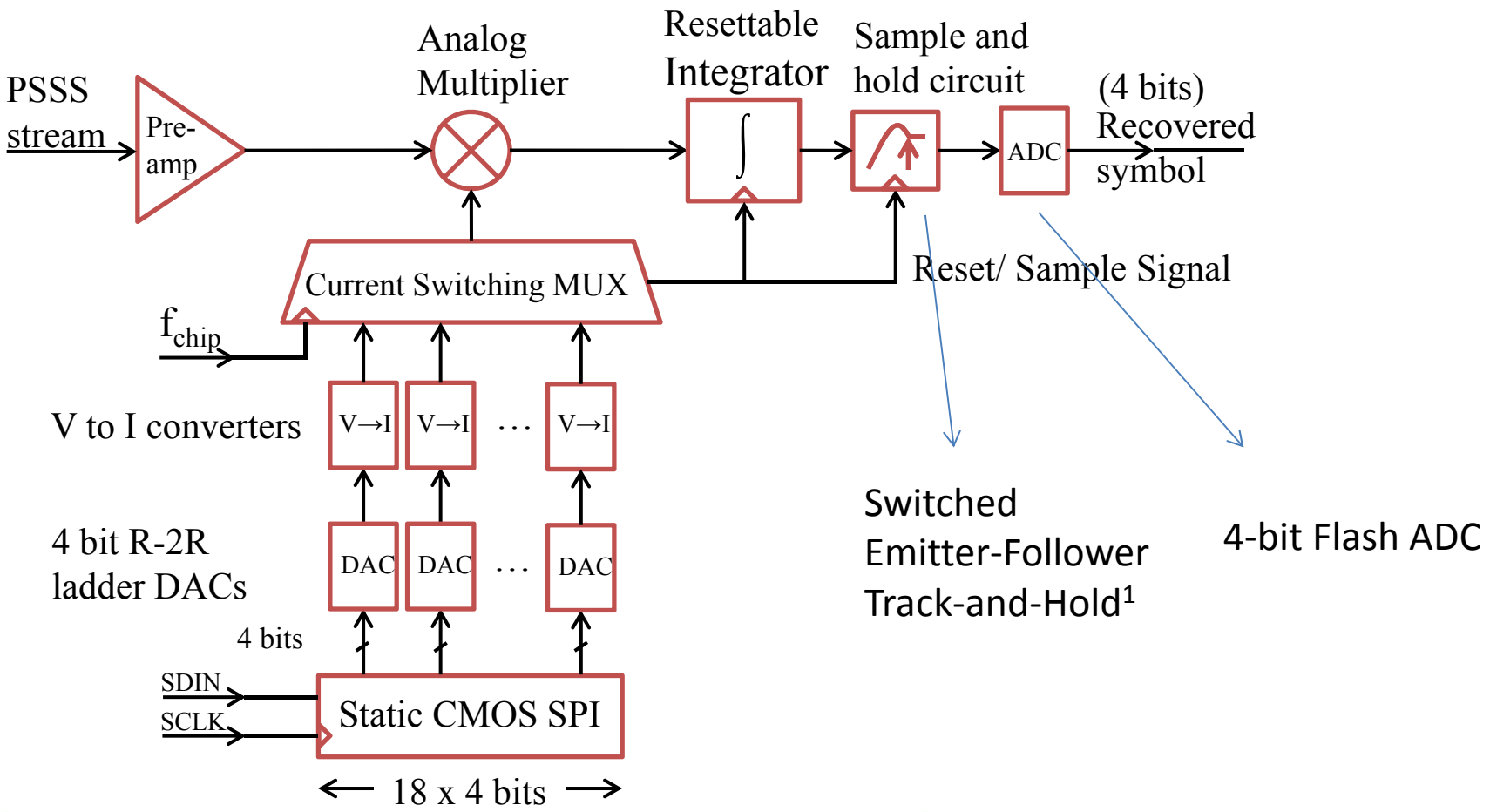




- Realized in 130 nm SiGe BiCMOS technology (SG13S) from IHP
- Measurement results show integrator step response and reset.
- Correlator with highest input bandwidth (>25 GHz) and smallest reset time (<130 ps) reported so far.

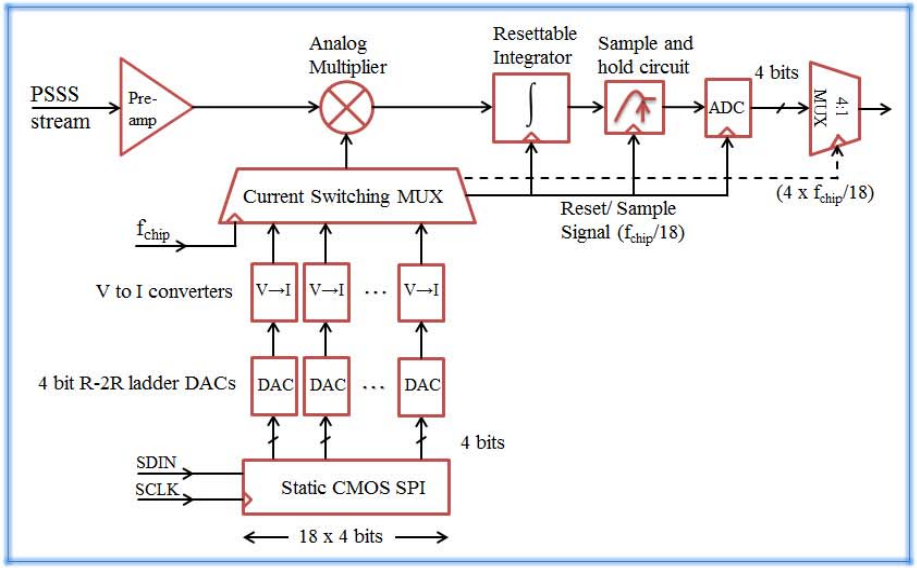
[1] A. R. Javed, C. Scheytt, U. v.d. Ahe: "Linear Ultra-Broadband NPN-only Analog Correlator at 33 Gbps in 130 nm SiGe BiCMOS Technology", IEEE BCTM 2016

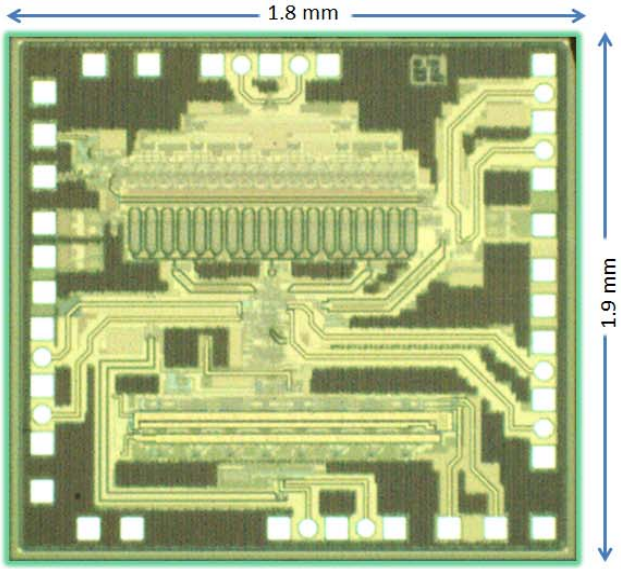
Integrate and Dump Correlator Circuit w. ADC



[1] similar to B. Sedighi, Y. Borokhovych, H. Gustat, C. Scheytt: "Low-power BiCMOS track-and-hold circuit with reduced signal feedthrough", IEEE IMS 2012

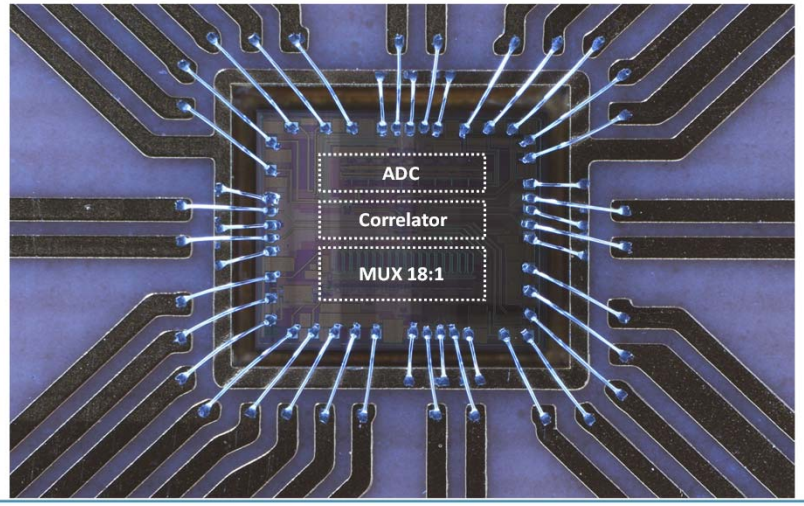
1 Channel PSSS Receiver Test Chip



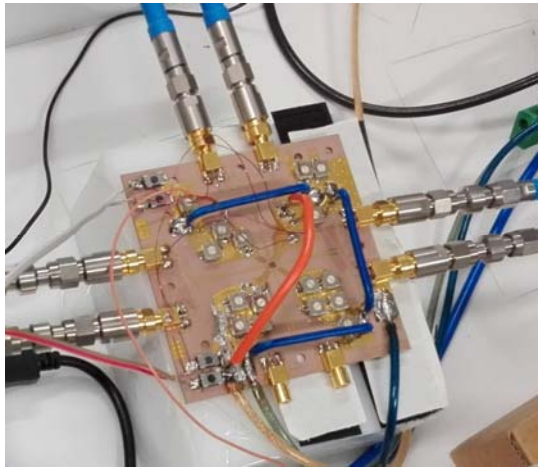


Serialized ADC Output

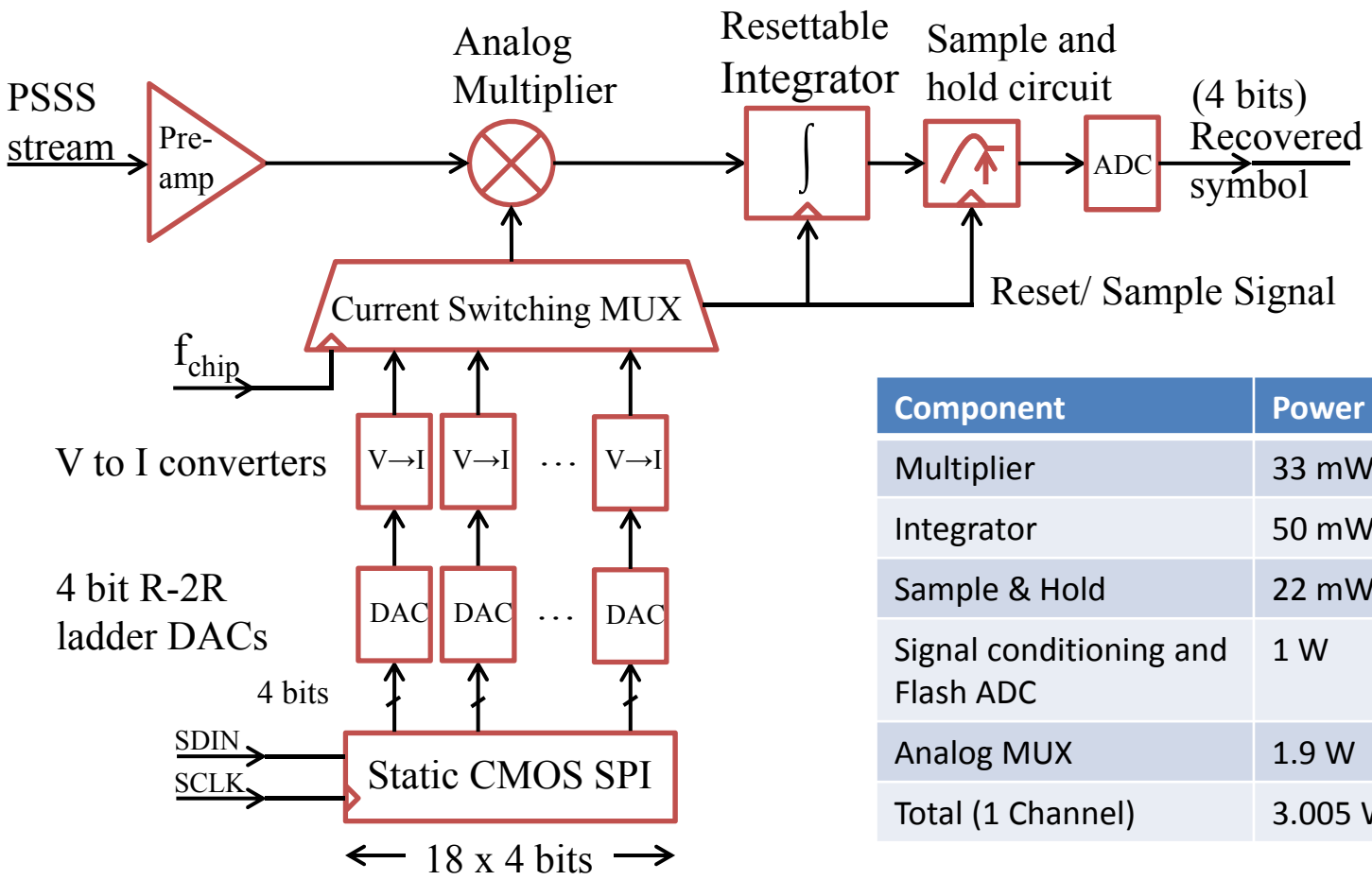
Correlator Output



PSSS Input



Power Dissipation



Component	Power diss.
Multiplier	33 mW
Integrator	50 mW
Sample & Hold	22 mW
Signal conditioning and Flash ADC	1 W
Analog MUX	1.9 W
Total (1 Channel)	3.005 W

- Circuit implemented in 130 nm SiGe BiCMOS. → high BW but not power efficient. Analog Current Switching MUX and Flash ADC most power hungry.

Conclusions

- 100 Gb/s wireless communication with high RF bandwidth (e.g. 50 GHz) has extreme demand wrt. to baseband data converters and signal processing.
- PSSS is an analog-friendly modulation scheme. Mixed-signal PSSS allows for data converters to operate on a fraction of the signal bandwidth and low sampling rate.
- Mixed-signal PSSS system design and link experiments were shown.
- Circuit design of critical components. Correlator with world‘s highest input bandwidth (>25 GHz) and smallest reset time (<130 ps) was demonstrated.
- Implementation in 130nm SiGe BiCMOS shows that a 100 Gb/s mixed-signal PSSS baseband is technically feasible, however not power-efficient.
- Power efficient implementation would require a CMOS implementation (at least 45nm) either mixed-signal or digital.