Development of Novel System and Component Architectures for Future Innovative 100 GBit/s Communication Systems

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Outline

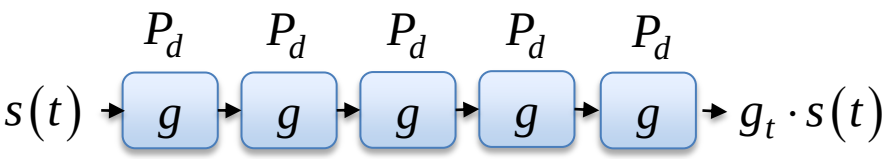
1. Introduction
   - Motivation
   - SPARS Concept
   - Transceiver Architecture
2. Project Topics
   - LHFT: System Concept Investigation and Experimental Verification
   - CCN: 180 GHz SPARS Receiver Frontend Design
   - LTE: 180 GHz QAM Modulator and High Speed DAC Design
   - INT: High Speed Receiver Analog Baseband Architectures and Design
3. Conclusion

Motivation

- High speed communication systems:
  - Symbol rate up to 20% of carrier
  - e.g. 2x18 GBaud at 180 GHz → > 100 GBit/s wireless
- Technological limitations:
  - Operation close to process transit frequency
    → Low single-stage amplifier gain
  - Scaling issues: Long amplifier chains, high area cost, high power dissipation
- **Goal: Scalable, efficient and broadband *quadrature* transceivers beyond homodyne architectures**

SPARS - „Simultaneous Phase and Amplitude Regenerative Sampling“ - A disruptive technology

The ordinary approach

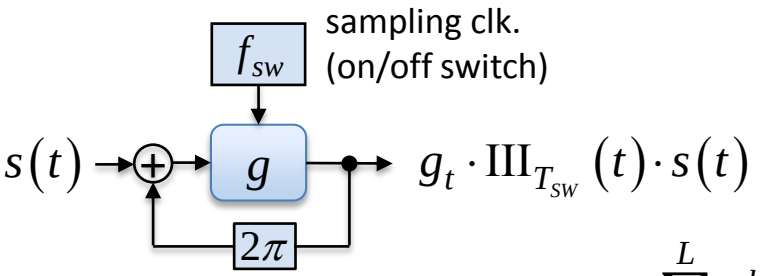


Gain: $g_t = g^N$

Example (with N=5; g = 2): $\Rightarrow \quad g_t = 32$

Power dissipation: $P_{d_{total}} = 5 \cdot P_d$

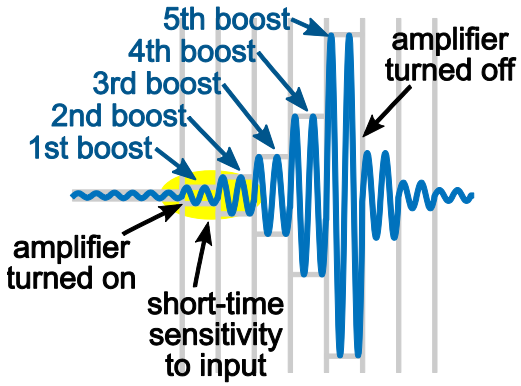
SPARS / SRO approach



Gain (*pos. feedback*): $g_t = \sum_{l=1}^{L} g^l$

Example: (with L=4; g = 2): $\Rightarrow \quad g_t = 30$

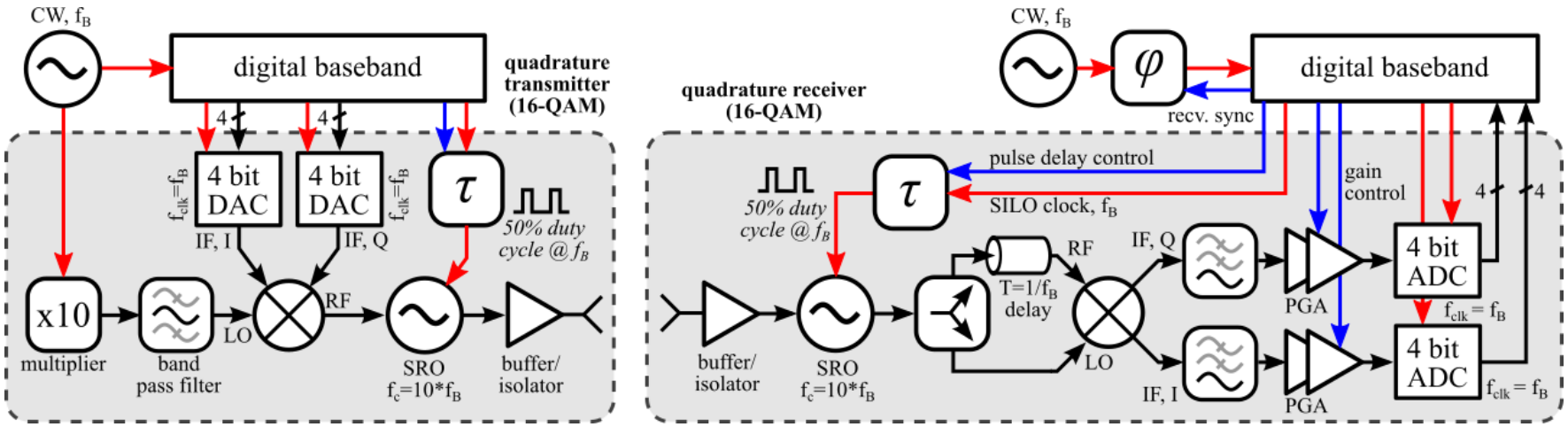
Power dissipation: $P_{d_{total}} = P_d$



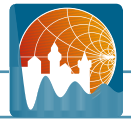
Power consumption and complexity dramatically reduced, especially useful when working close to transit frequency

System Concept

- Novel Transceiver Architecture: „SPARS“, *Simultaneous Phase and Amplitude Regenerative Sampling*
- Major Benefits: Overcome scaling and power dissipation issues by:
  - High gain boost with single stage amplifier (6 dB → 30 dB)
  - No PLL, no stabilized LO, no LNA or PA chains
  - Employing self-mixing receiver approach
  - Relaxing modulator power level requirements



System Concept Investigation and Experimental Verification



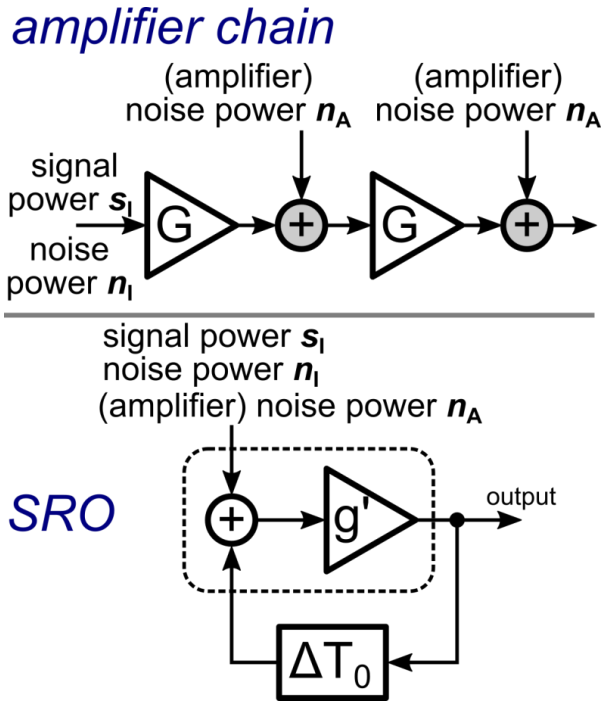
Noise Figure, SNR/Sensitivity

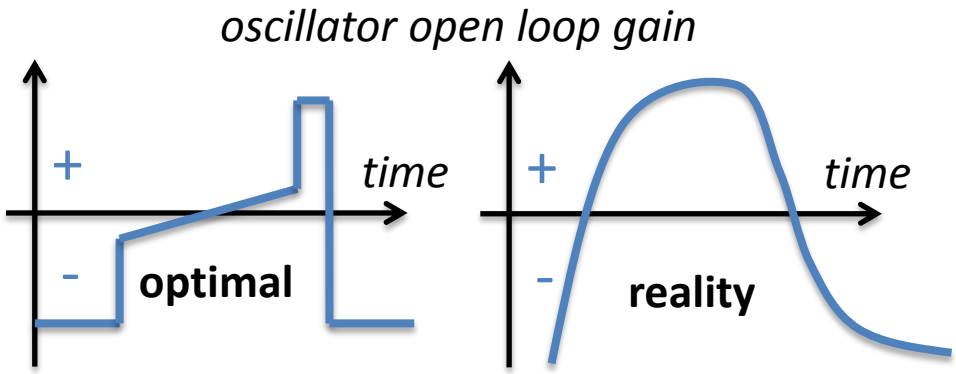
- Super-regenerative oscillator vs. amplifier chain
- Difference:
  - amplifier chain adds noise after each stage:
  - SRO adds signal **and** noise at each oscillation cycle:

$$F_{ac} = F + \sum_{k=1}^{n-1} \frac{F-1}{G^k}$$

$$F_{sro} = F$$

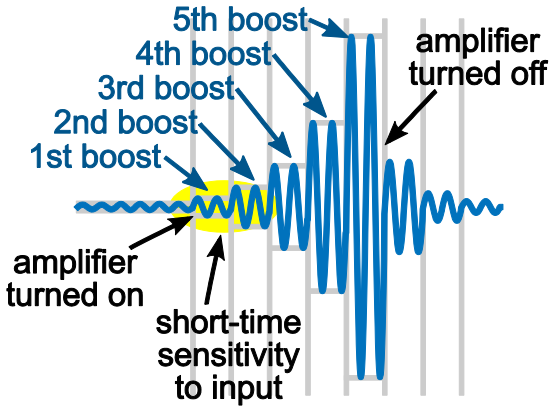
- Noise bandwidth?
  - homodyne receiver: symbol rate is lower bound (with sinc-shaped pulses, rect. filter)
  - super-regenerative theory: → similar performance achievable
  - at technological boundaries: 2-4 dB excess
- **overall: SRO and amplifier chain comparable / slight SRO advantage**

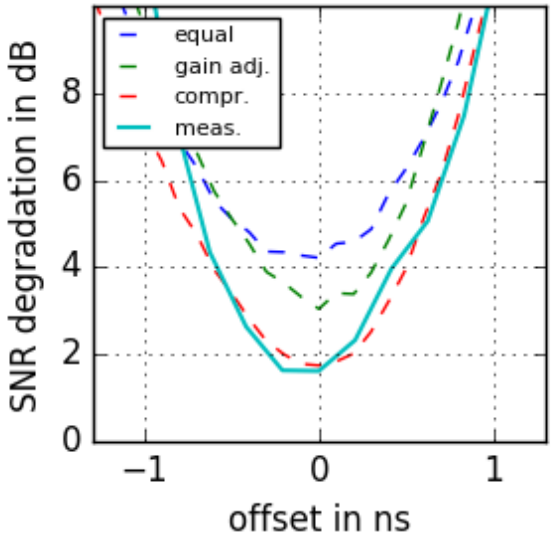


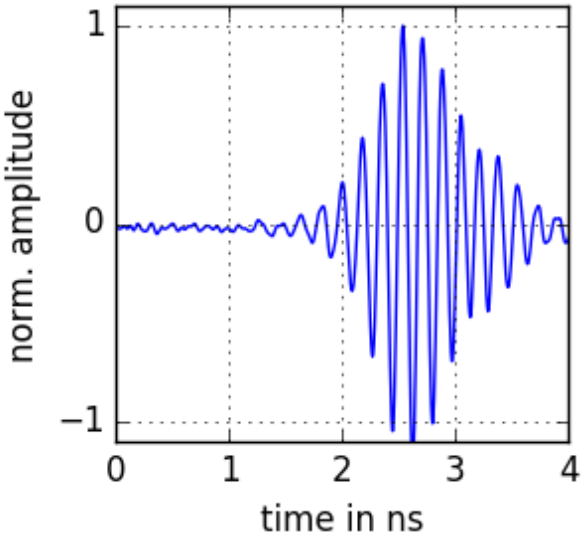


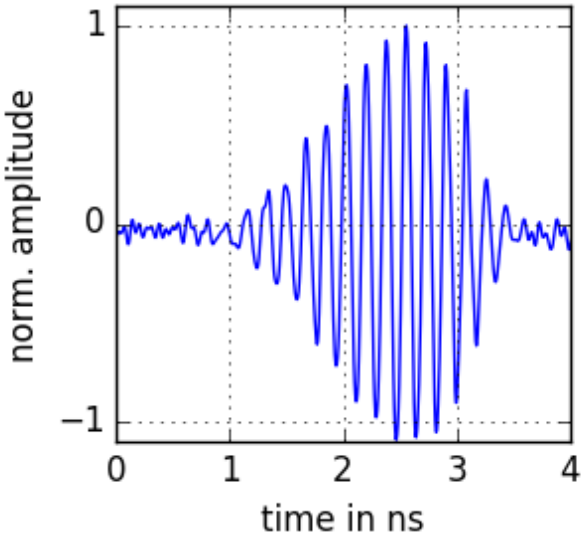
Pulse Recovery

- SRO samples *average* input power during sensitivity phase
- countermeasures (if peak power limited):
  - gain tuning → faster rise, shorter sampling period
  - slight compression → widens peak maximum
  - quench signal shaping → hold unity gain on decay



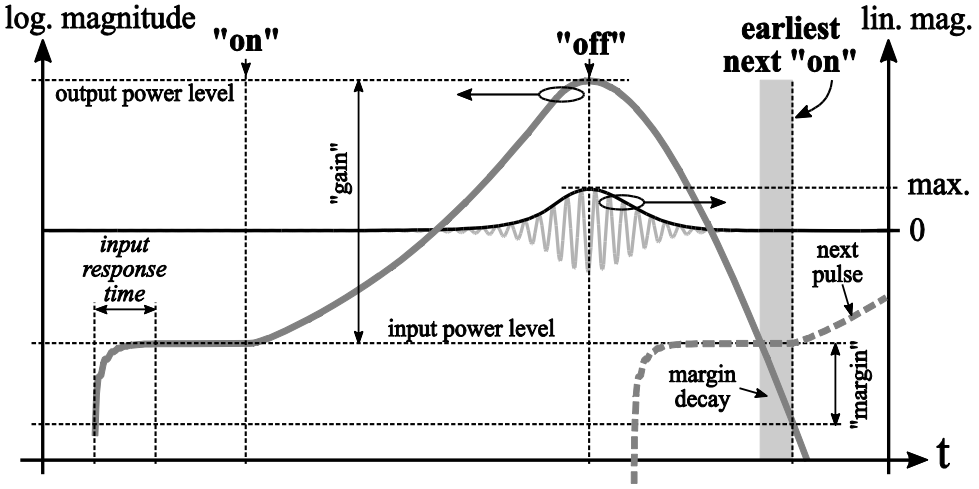


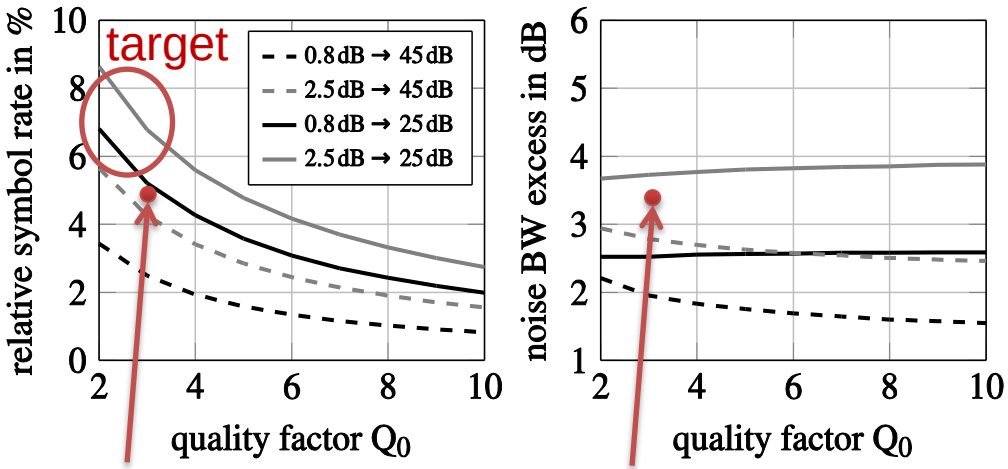




Achievable Data Rate

- Minimum period: Oscillation rise and decay + SNR margin
- Dependencies:
  - oscillator tank quality factor Q_0
  - active element gain M
- Typically low open loop gain (e.g. < 3 dB)
- Rise time limitation ($\tau=2/f_0 \ldots 4/f_0$) included in simulation
- Results:
  - 10x gain with 8-10% relative symbol rate could be achieved
  - Preliminary experimental result with scaled demonstrator
    - 270 MBaud measured @ 5.8 GHz
    - 293 MBaud theoretical expectation

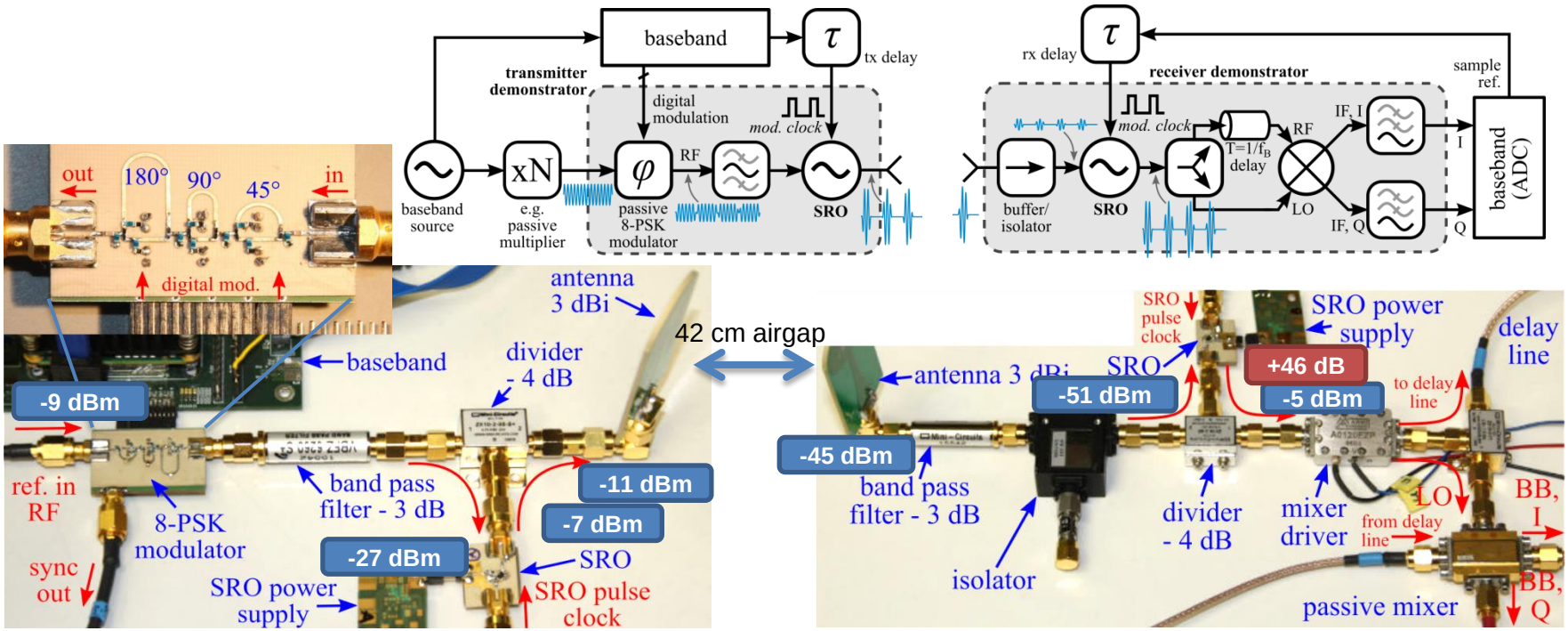




preliminary experimental results (scaled demonstrator)

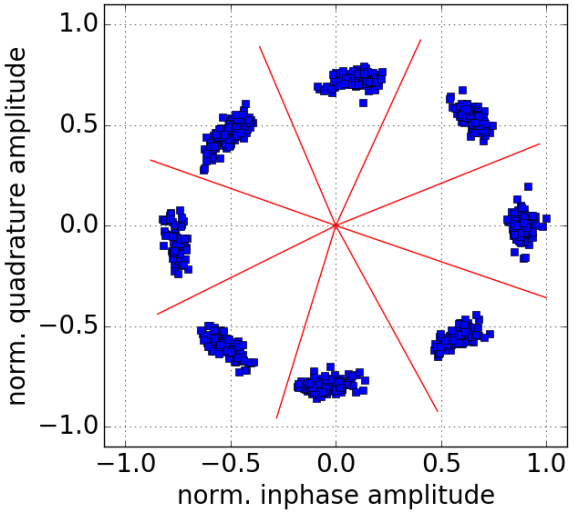
Demonstrator Implementation

- Complete transmitter and receiver at 5.8 GHz, 150 MBaud (450 MBit/s)
  - passive 8-PSK modulator (diode switched transmission lines, 11 dB loss)
  - discrete SRO (electrically small, single port)
  - filter/antenna from COTS components (~10 dB loss)
  - Receiver: Isolator at input, self-mixing with cable delay line

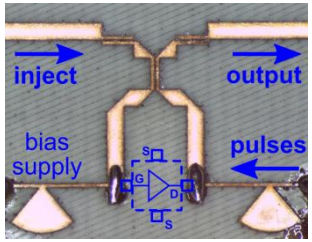


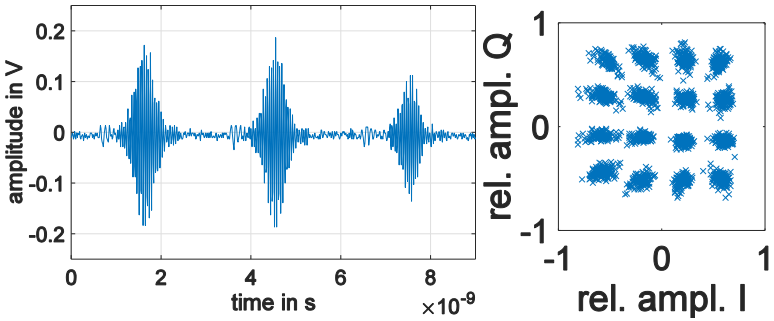
Demonstrator Measurement Results

- Complete Transmitter & Receiver:
  - Modulation: 8-DPSK
    - EVM < -18 dB (BER < 10^{-3})
    - diff.: EVM < -21 dB
  - Measured Deviations:
    - TX EVM -30 dB (systematic)
    - RX EVM -24 dB (stochastic)
  - Sensitivity CW: -77 dBm, pulsed: -75 dBm
    → close to theoretical SNR=P_s/(k*T*B*F)

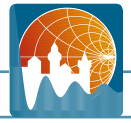


- 24 GHz 16-QAM Demonstrator (SRO only):
  - 343 MBaud (1.37 GBit/s)
  - 5 dB single stage gain
    → 25 dB
  - linear recovery of amplitude and phase



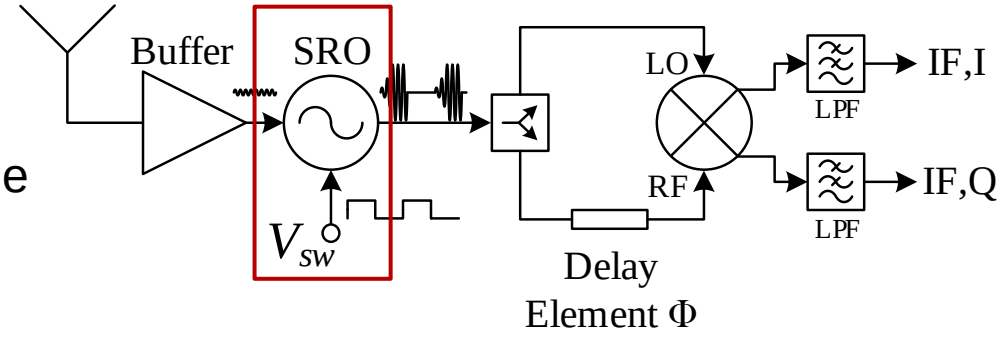


180 GHz SPARS Receiver Frontend Design

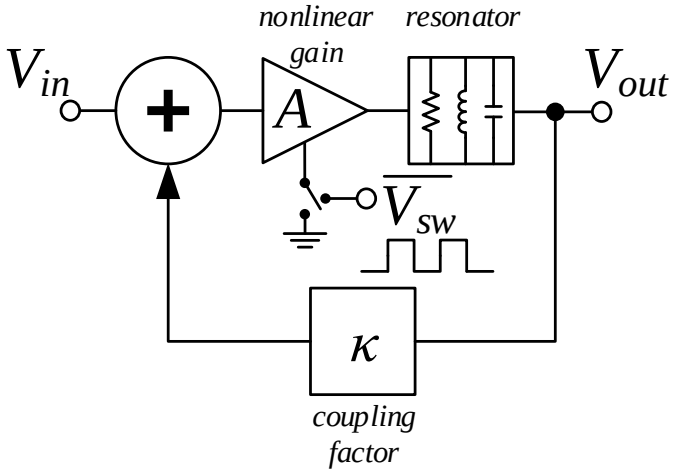


Integrated mm-Wave Super-Regenerative Oscillators (mmW SROs)

- Most amplification is done in SRO component
- Many design compromises possible e.g. gain, symbol rate, dynamic range, etc.
- Proper modelling of SRO circuit provides guidelines for performance optimization
- Large-signal behavior is of highest importance
- Study relation between V_{out} and V_{in} in phase and amplitude
- Model implemented electrically using CAD tools
- Cross-coupled topology chosen for monolithic integratibility

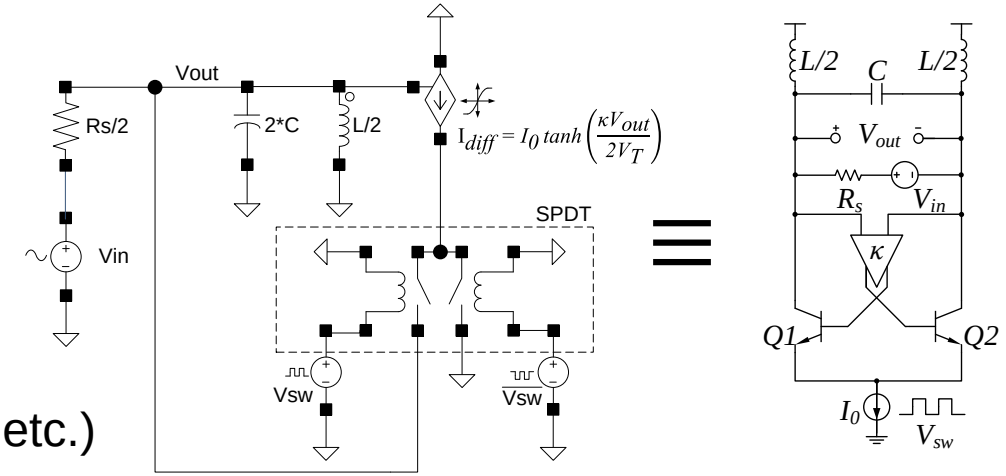


Proposed Regenerative Receiver

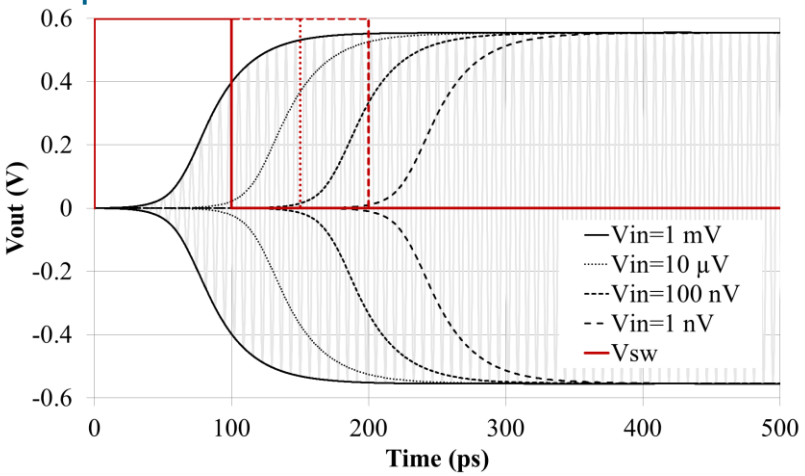


Modeling of integrated mmW SROs

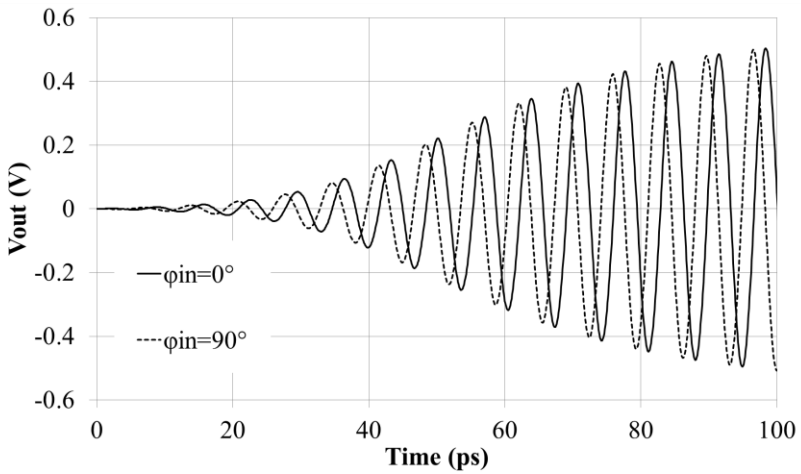
- Ideal nonlinear model; no base currents, numerical simulations
- Amplitude and phase sampling
- Influence of design variables on performance can be studied (e.g. loop gain, RC time constant, etc.)



Amplitude Modulation

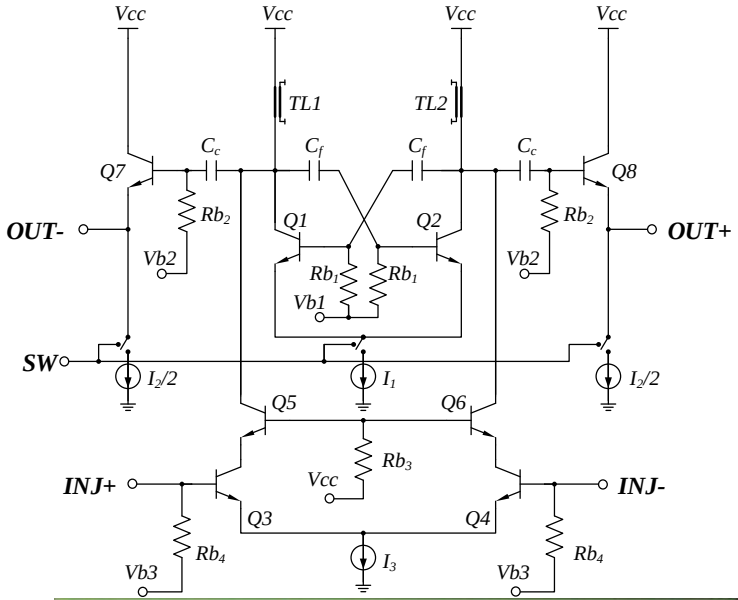


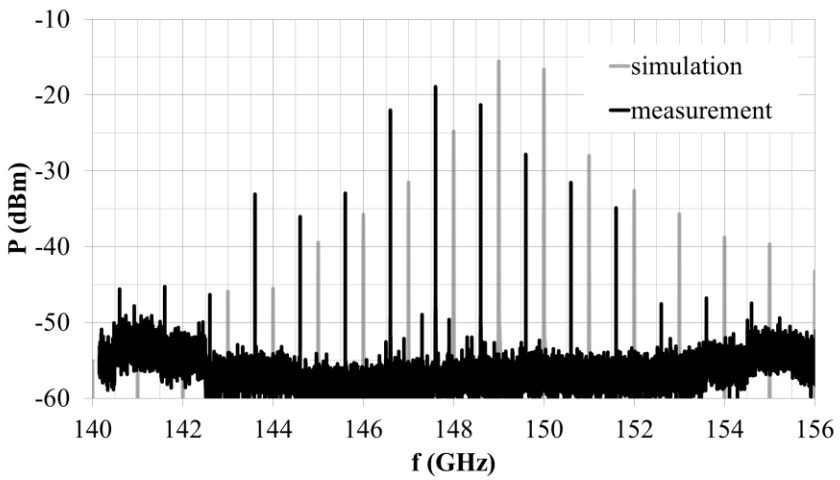
Phase Modulation

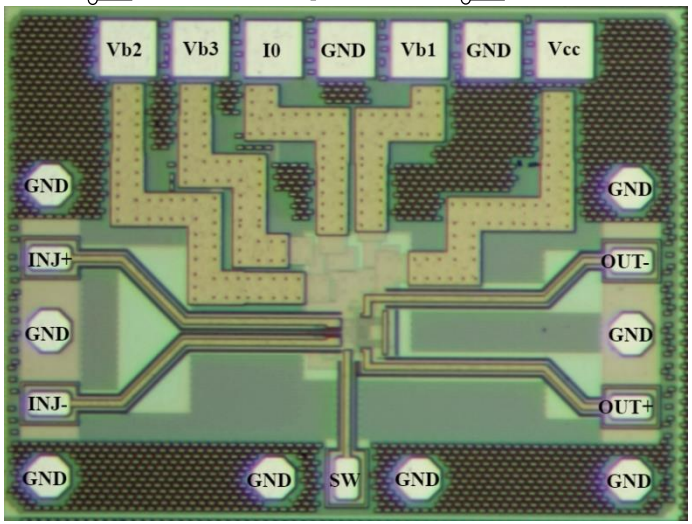


Cross-Coupled mmW SRO in IHP 0.13-µm SiGe BiCMOS

f_{osc} (GHz)	148
P_{DC} (mW)	48
f_{sw} (GHz)	1
P_{out} (dBm)	-6
Area (mm²)	0.66
Gain (dB)	36

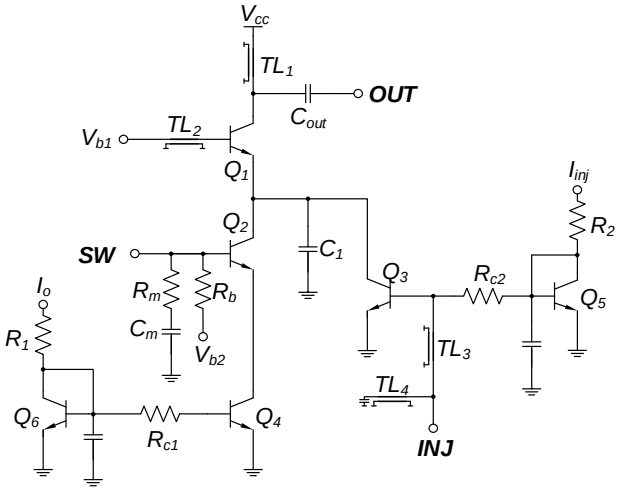


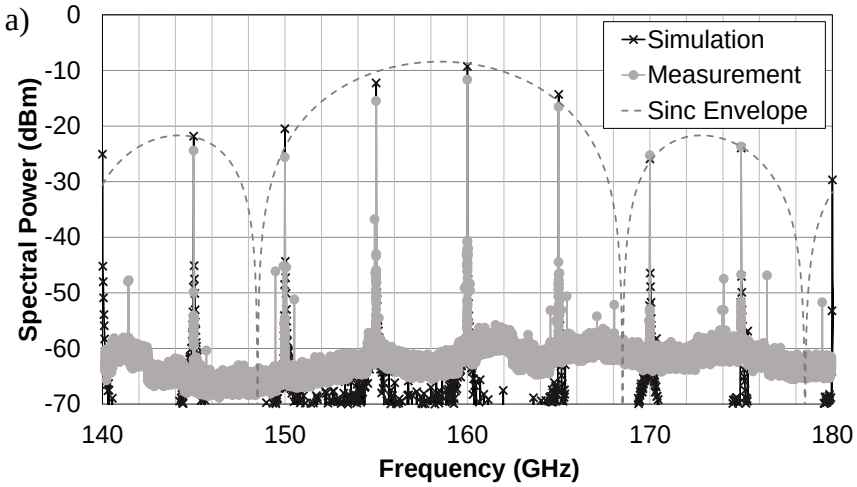


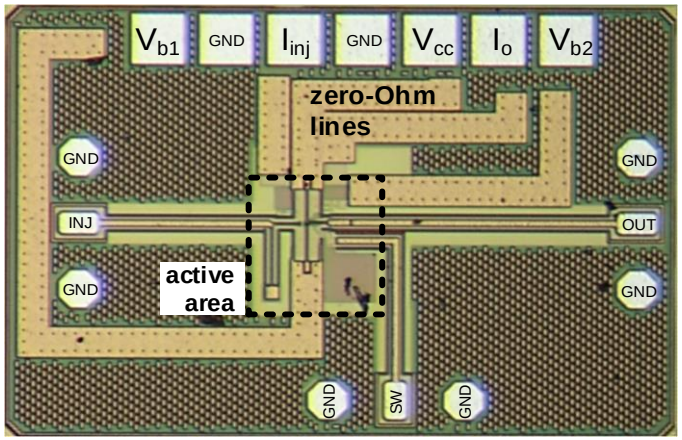


Single-Ended Colpitts mmW SRO in IHP 0.13-µm SiGe BiCMOS

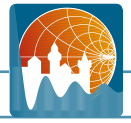
f_{osc} (GHz)	160
P_{DC} (mW)	6.6
f_{sw} (GHz)	5
P_{out} (dBm)	-8.4
Area (mm²)	0.64
Gain (dB)	18.4



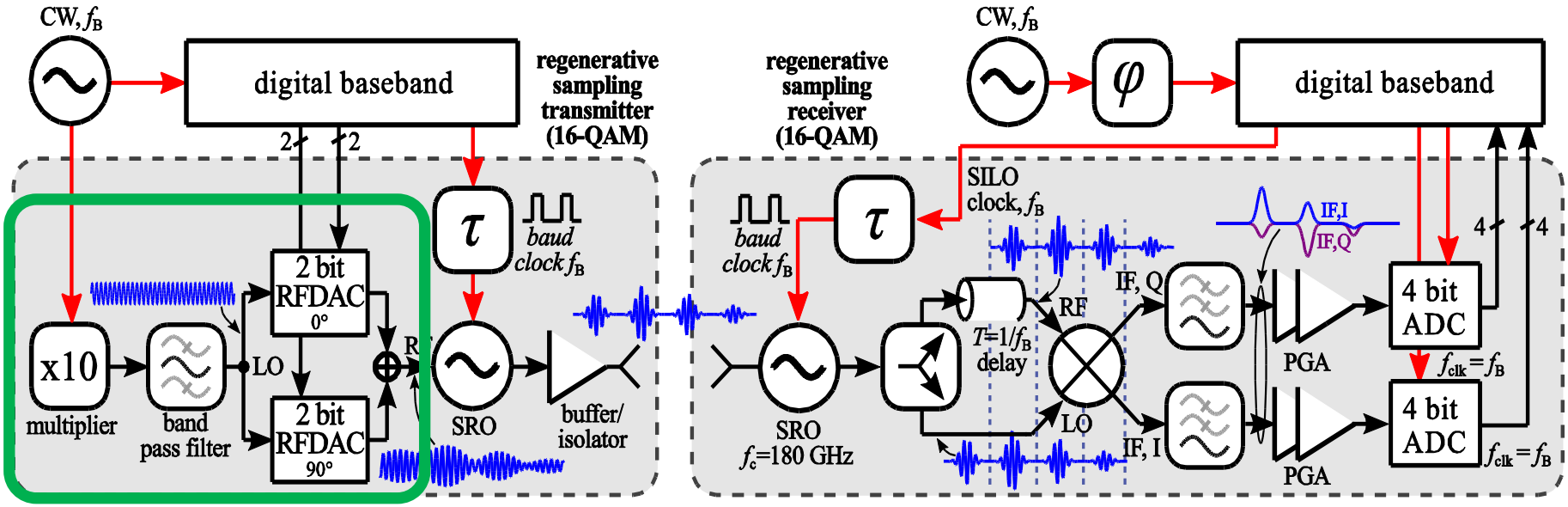




180 GHz QAM Modulator and High Speed DAC Design



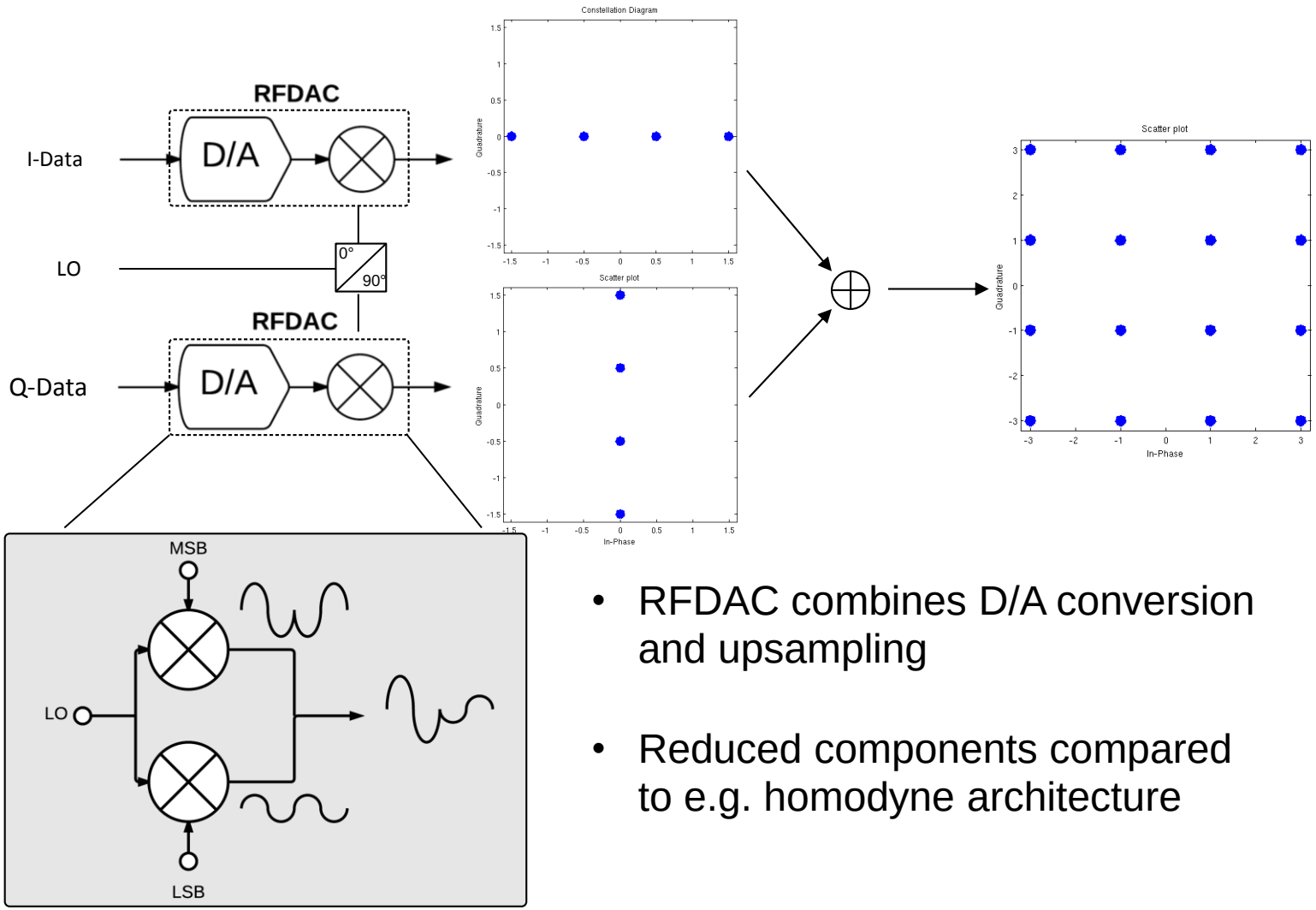
SPARS based frontend



Functionality

- Generates 180 GHz carrier frequency with a times ten frequency multiplier
- 16 QAM modulation achieved via two radio-frequency Digital-to-Analog Converters of 2 bit each with a modulation rate of up to 18 GS/s

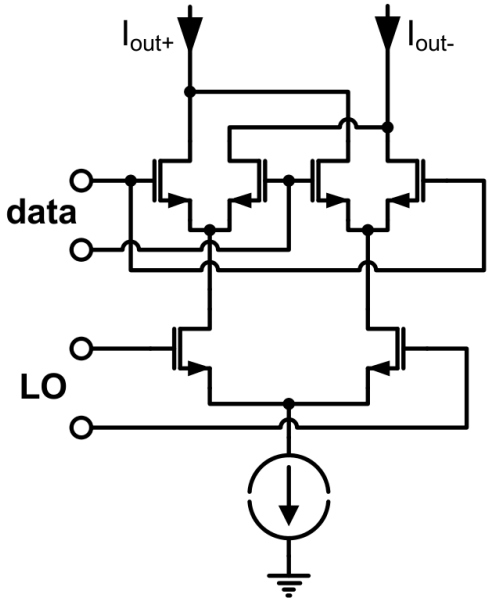
Radio-Frequency Digital-to-Analog Converter



- RFDAC combines D/A conversion and upsampling
- Reduced components compared to e.g. homodyne architecture

Radio-Frequency Digital-to-Analog Converter

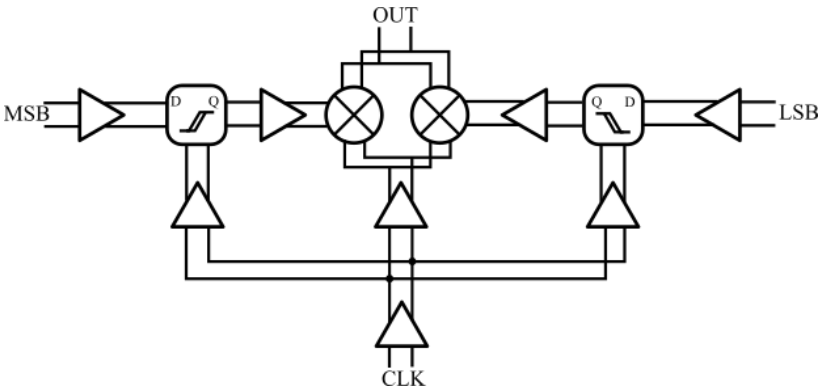
- Current steering principle
  - Better spectral purity and wider bandwidth
- Upsides
  - Rejection of all outputs at DC and even harmonics of f_{LO}
  - All transistors act as switches, hence no linearity constraints
- Linearity of output signal defined by:
  - Resolution of converter
  - Output impedance modulation
  - Mismatch in timing



Example of RF-DAC output stage

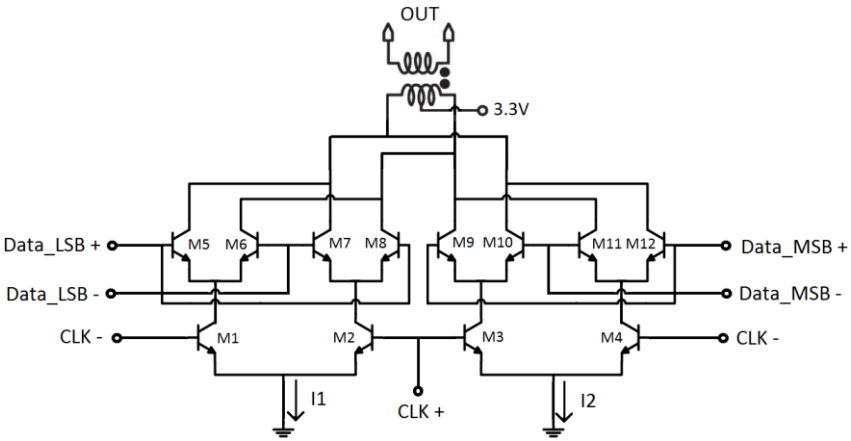
Design of a 2 bit 180 GHz RF-DAC for SPARS

- Each RF-DAC consists of three identical RF-DAC cells
  - Current summation at the output via broadband transmission lines
  - Buffers for signal boosting and for blocking of clock feed through
  - Flip-Flops for retiming purposes



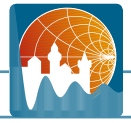
RF-DAC Cell

- Output stage of each RF-DAC cell features two parallel connected Gilbert cells working as BPSK modulators
  - Ratio between the transistors and currents of the two Gilbert cells to be 3:1
  - Transformer increases linearity and SNR

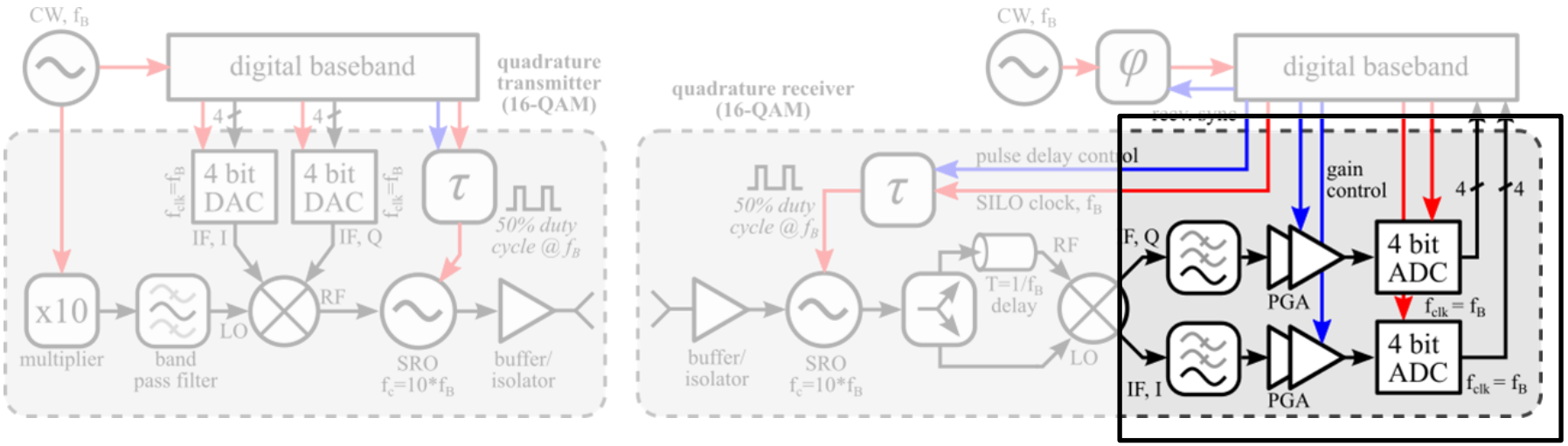


RF-DAC output stage

High Speed Receiver Analog Baseband Architectures and Design



SPARS baseband receiver



Analog baseband receiver

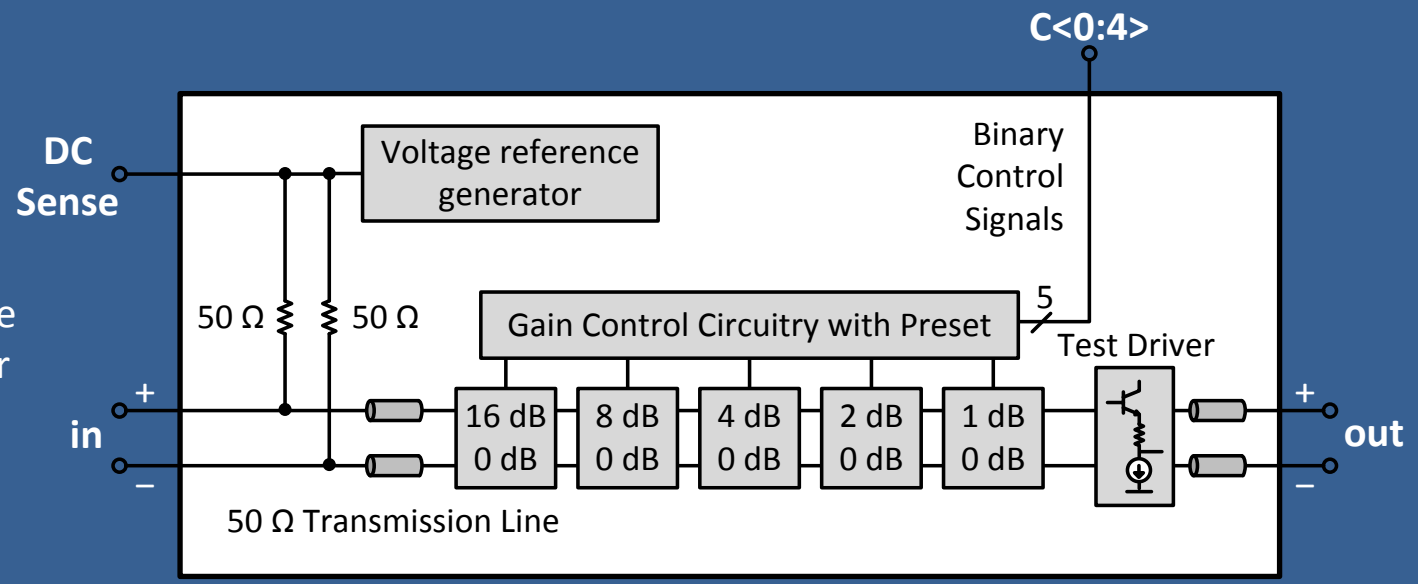
Functionality

- Digitization of wideband inphase (I) and quadrature (Q) receive signals (> 9 GHz) by **PGA+ADC solution**
- **External data storage on FPGA** to ensure a sufficient number of receive samples for
  - system demonstration experiments and
  - evaluation of link synchronization parameters (e.g., I/Q gain and phase mismatches, etc.)

SPARS PGA

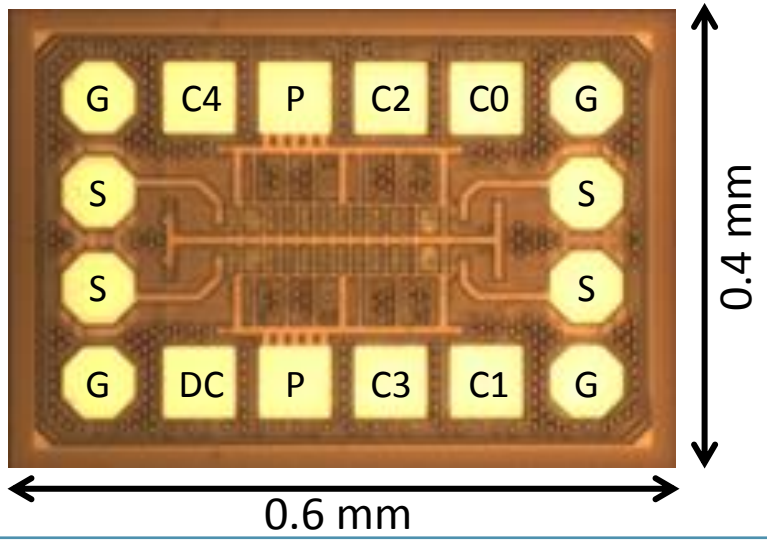
PGA architecture

PGA . . . Programmable Gain Amplifier



Die photograph

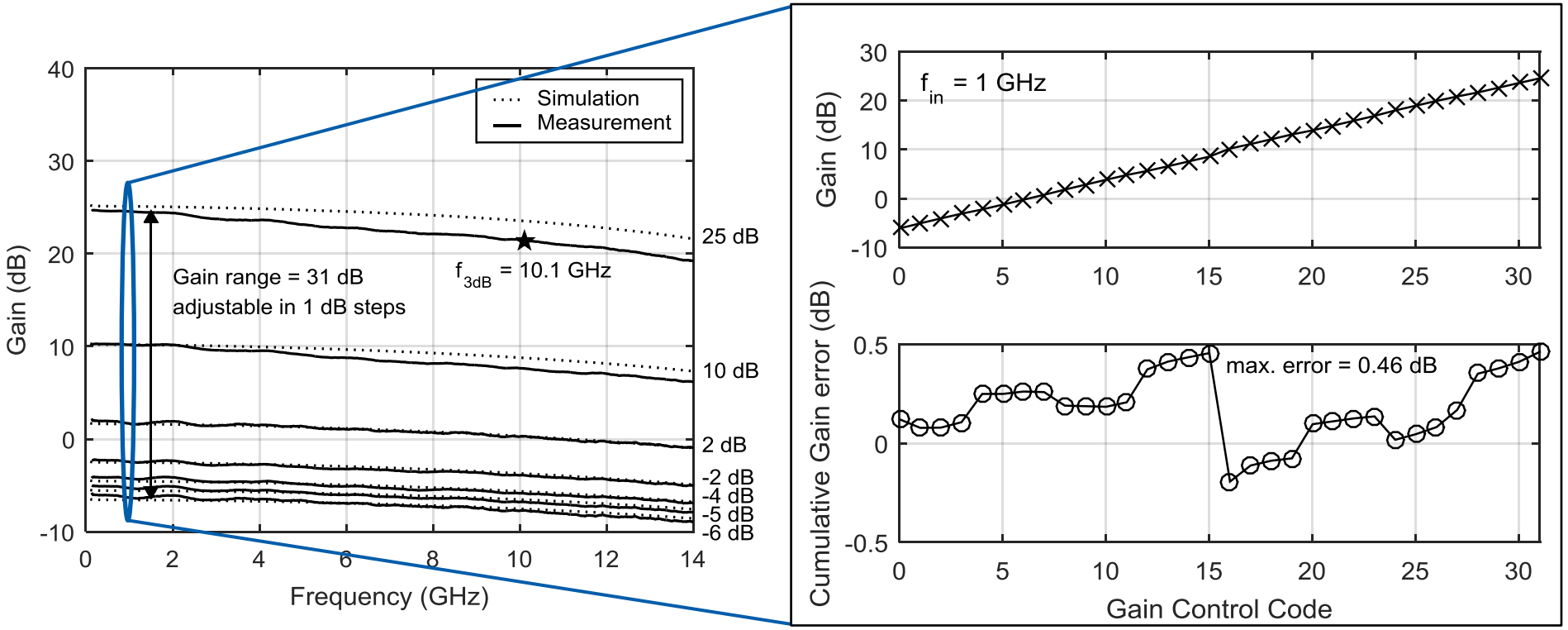
implemented in 0.13 µm SiGe BiCMOS from IHP



Specifications

Gain range:	31 dB in 1 dB steps
Gain accuracy:	-0.19/0.46 dB @ 1 GHz
Bandwidth:	>10.1 GHz

Measurement Results



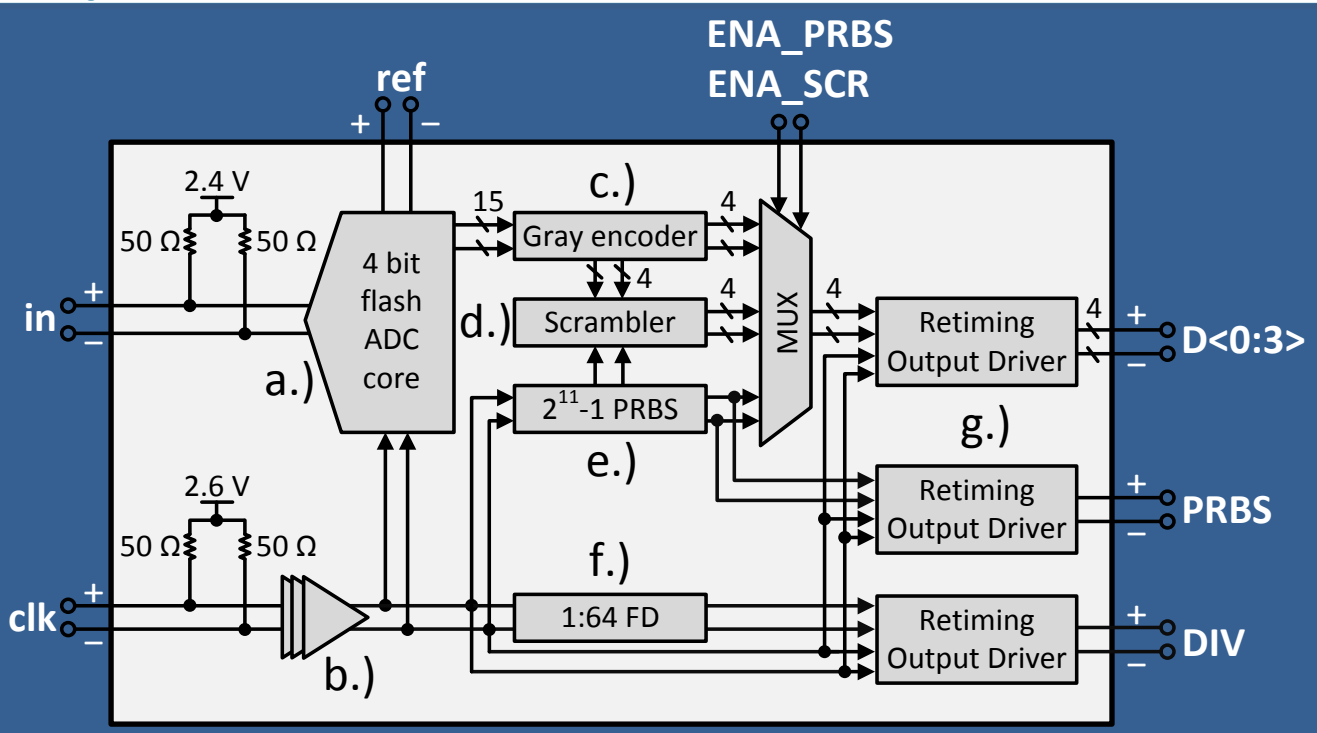
Achievements

- **Low-complexity** PGA architecture
- **31 dB gain range** programmable in **1 dB steps**
- Gain accuracy smaller than 0.46 dB
- **>10.1 GHz 3-dB bandwidth**

SPARS ADC

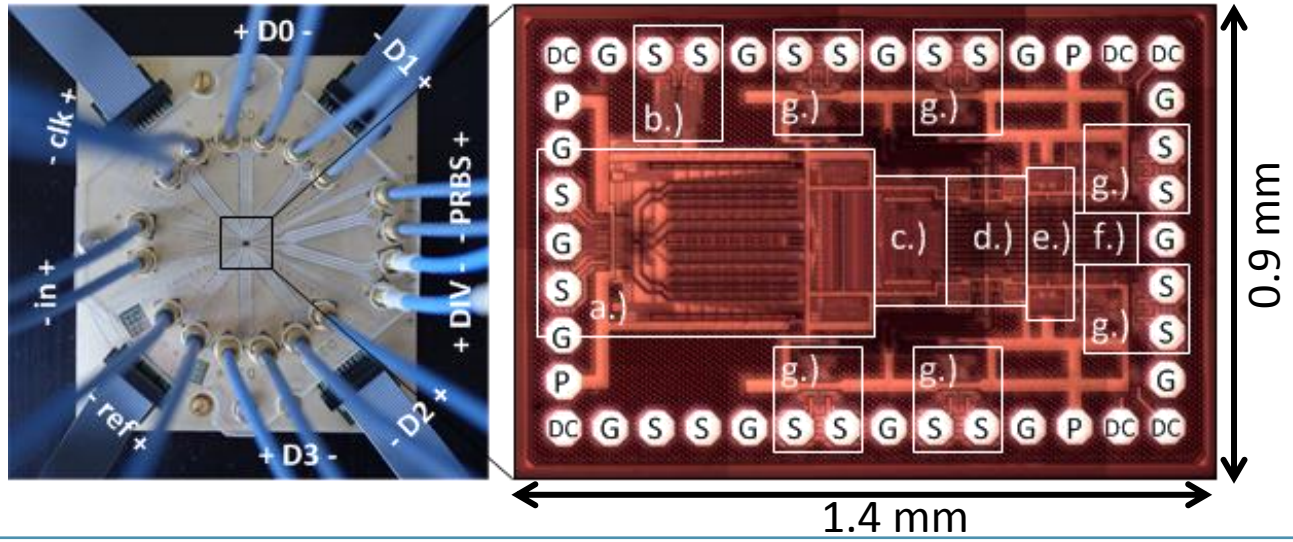
ADC architecture

ADC . . . Analog-to-Digital Converter
PRBS . . . Pseudo Random Bit Sequence
FD . . . Frequency Divider

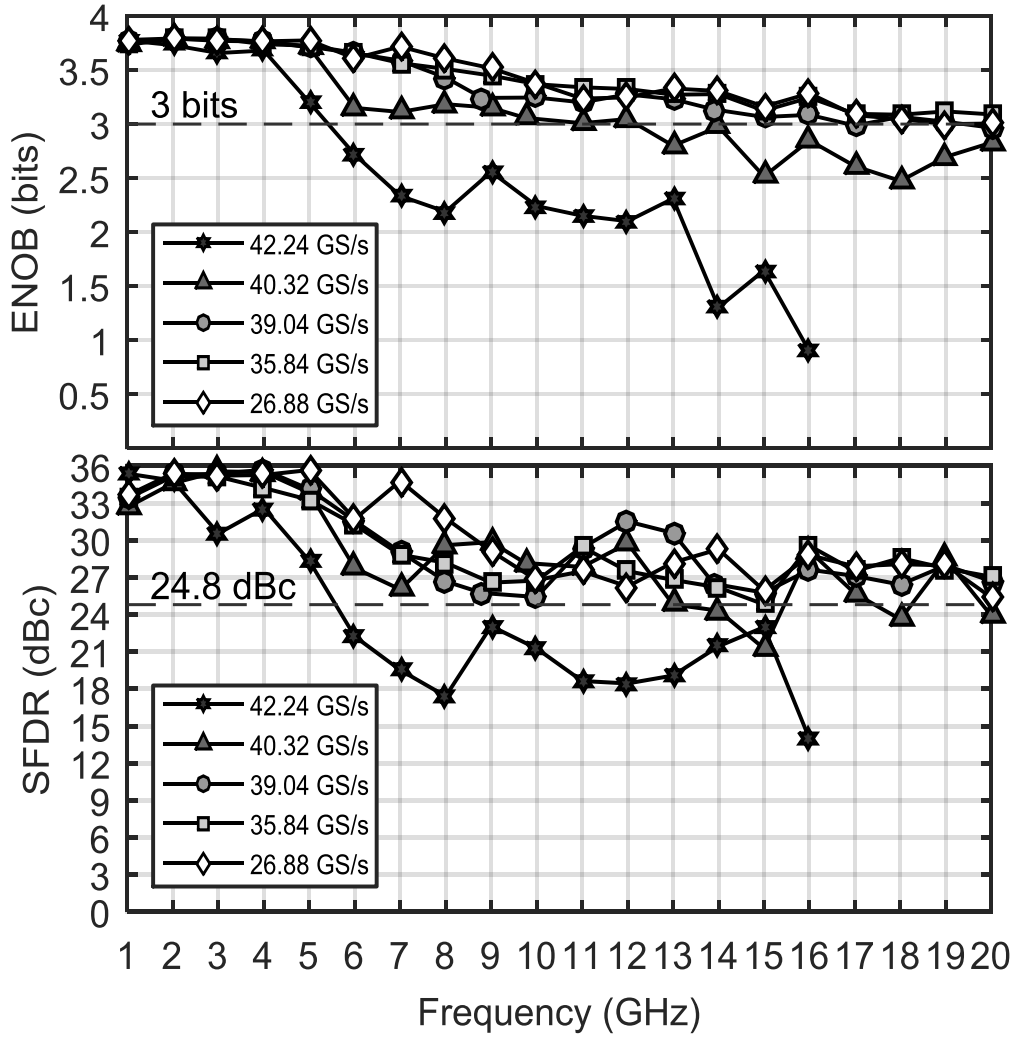


RF PCB (left) and die photo-graph (right)

implemented in 0.13 µm SiGe BiCMOS from IHP



Measurement Results



Achievements

- Enables sampling rates from DC to 42 GS/s
  => more than **60% speed improvement** to current state-of-the-art single-core ADCs with digital encoder (25 GS/s)
- **ENOB > 3 bits** and SFDR >24.8 dBc within **DC-20 GHz frequency band** up to 39 GS/s
- FOM = 8.3 pJ/conv.

FOM . . . Figure of Merit

Real-time measurement with 70 GHz sub-sampling scope

Conclusion

- Novel transceiver architecture concept based on „Simultaneous Phase and Amplitude Regenerative Sampling“
  - significantly reduced system size and power consumption (single-stage instead of multi-stage amplifiers, no receiver synthesizer, …)
  - verified to be competitive to homodyne system in terms of noise and data rate with scaled demonstrator
- mmW Super-Regenerative Oscillator for 180 GHz target frequency implemented and successfully verified
- Transmitter RFDAC concept investigated and implemented to exploit relaxed power level requirements from high SRO gain
- 4 bit ADC with up to 42 GS/s and outstanding performance as well as wideband baseband PGA demonstrated experimentally
- Next steps: Component integration to demonstrate mmW self-mixing receiver

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