WS 03 - Wireless 100Gb/s and beyond: Progress in ultra-fast wireless communications

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Challenges and potential solutions for wireless 100Gb/s communication systems

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Outline

1	What is a DFG-SPP?
2	SPP1655: „Wireless 100 Gb/s and beyond"
3	"Bandwidth Efficiency" versus "Bandwidth"
4	"Digital Signal Processing" versus "Analog Signal Processing"
5	"Protocol Design Challenges"
6	Conclusion

## What is a DFG SPP (Special Priority Program)?

Purpose:

- Advance knowledge in an emerging field of research through collaborative networked support
- Enhanced quality of research through the use of new methods basic science
- Added value through interdisciplinary cooperation
- Collaborative networked support over several locations national wide
- Researchers prepared call approved by the DFG-senate

Eligibility: Researchers at universities research institutions in Germany

Funding period: 6 (3 + 3 or 3*2) years

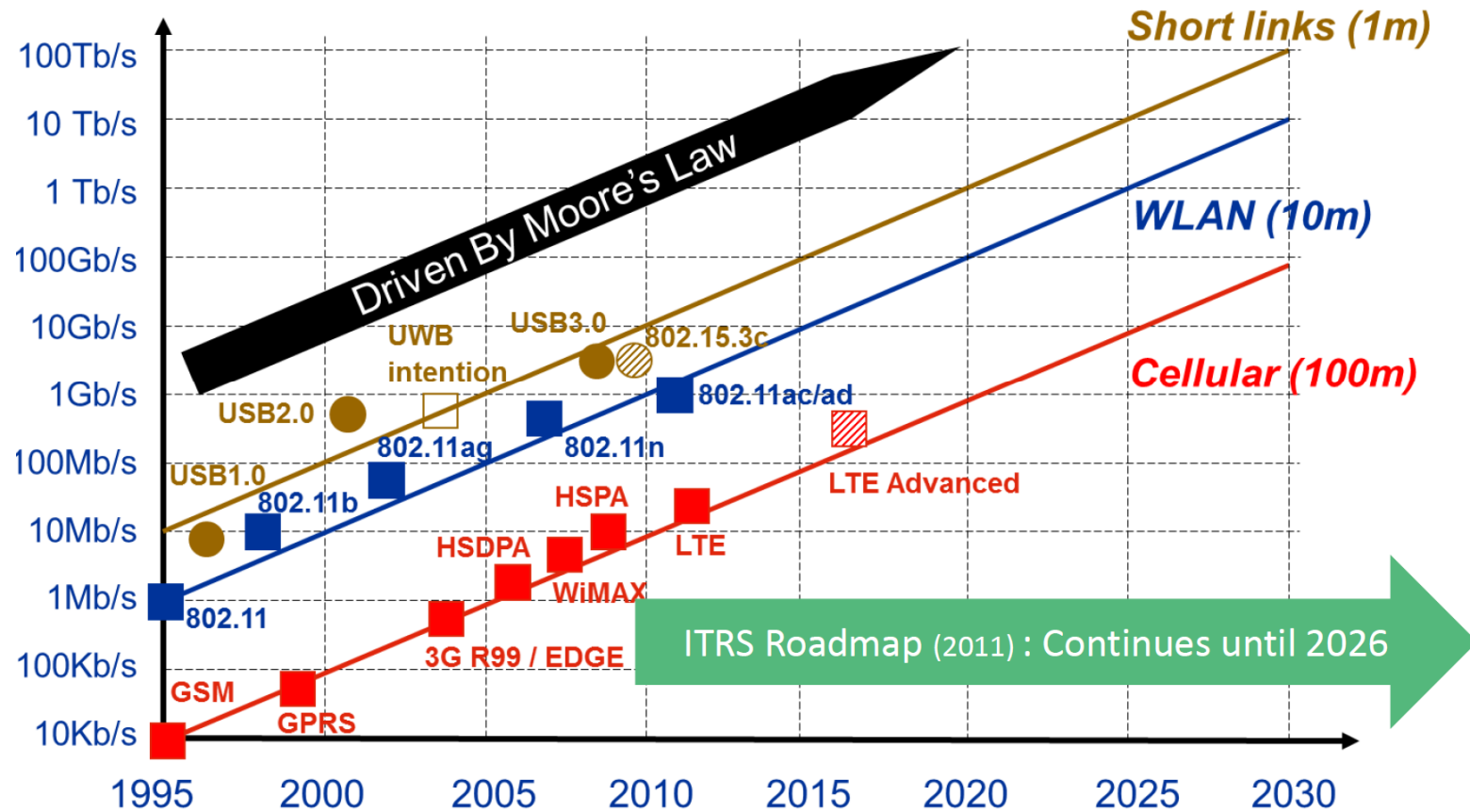Funding: individual grants + coordination (~ 30 PIs)
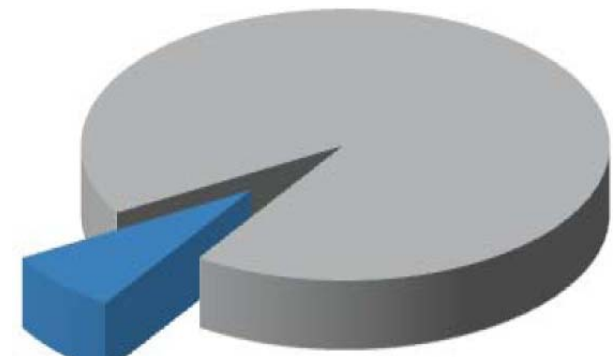
7.5% of budget for SPPs

Slide borrowed from Dr. Damian Dudek DFG

Wireless Roadmap (Fettweis 2012)

The Wireless Roadmap

Objectives of „Wireless 100Gb/s and beyond"

- Investigation of paradigms for effective reduction of complexity and energy consumption of ultra-high speed wireless communication systems

  - We need to come close to 1-10 pW/b for the end-2-end communication

- Comparison of baseband algorithms with respect to bandwidth efficiency and energy efficiency

- Investigation of the boundary between digital and analog signal processing

- Investigation of medium access protocols for systems with ultra-high speed, significant error handling and low energy

- Investigation of Silicon based transistors with cut-off frequencies of 700 GHz and higher

- Investigation of system architectures (including protocols) for extreme high data throughput

Bandwidth Efficiency versus Bandwidth

Basically 2 cases are discussed:

- Use a huge bandwidth at a very high frequency with a small bandwidth efficiency (50GHz, 250GHz, 2 b/s/Hz) or
- Use a small bandwidth with a huge bandwidth efficiency at a moderate frequency (3GHz, 7GHz, 33 b/s/Hz)

What SNR do we need in different cases of bandwidth efficiency to achieve 100Gb/s

According to Shannon $S/N_0 = 2^{\eta}-1$ with $\eta=C/B$ we need as a minimum:

- For System 1: f=250GHz B=50GHz η=2 b/s/Hz.
- i.e. for S/N_0 we need a minimum of 4.7 dB with
- $N_0=4kTB=4*300*50*10^9*1,38*10^{-23}J/s=0,83*10^{-9}W$
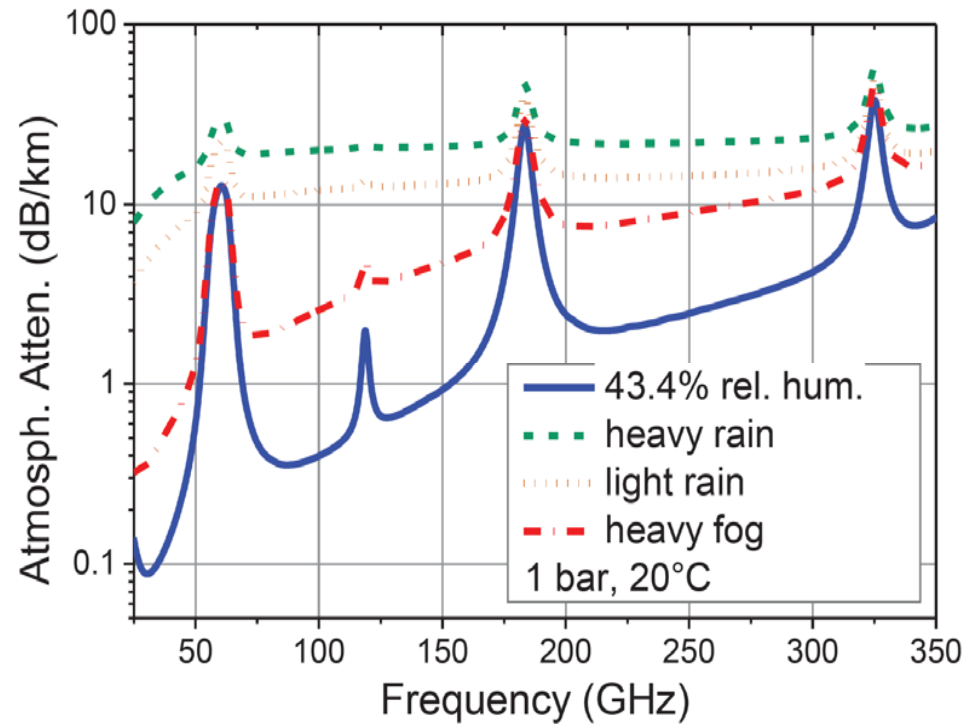
- For System 2: f=7GHz, B=3GHz η= 33 b/s/Hz
- i.e. for S/N_0 we need a minimum of $2^{33}-1=$ $8*10^9$ or 108dB
- $N_0=4kTB=4*300*2*10^9*1,38*10^{-23}J/s=0,03*10^{-9}W$
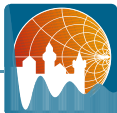
Ultra high frequency challenges

- Free space losses grow with the square of the frequency
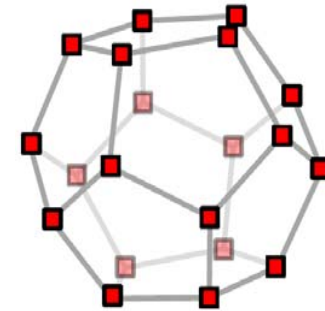- Atmospheric losses limit the transmission distance significantly

$$P_R = P_T G_T G_R \left(\frac{\lambda}{4\pi r}\right)^2$$
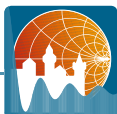
Bandwidth Efficiency versus Bandwidth
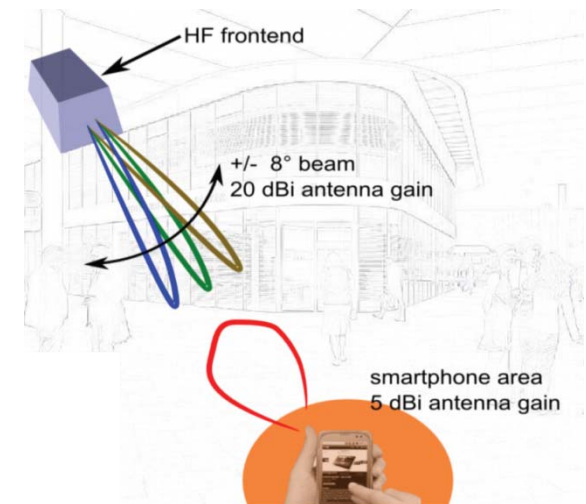
We cannot achieve such a high bandwidth efficiency using just one channel

- Thus parallelization (e.g. MIMO) is absolutely necessary
- "Massive MIMO" might be a way to go

For ultra high frequencies the free propagation loss is huge

- Thus we need highly directed antennas with gains of >30dBi

HF frontend

+/- 8° beam
20 dBi antenna gain

smartphone area
5 dBi antenna gain

Digital Signal Processing" versus "Analog Signal Processing

Digital Case:

- For a normal IEEE802.11n system (300Mb/s) we need a DSP performance of approximately 2 GFLOPS (mainly for FEC and MIMO processing).

- The bandwidth efficiency of IEEE802.11n is at maximum η=15 (b/s)Hz.

- The energy consumption per MFLOP at a 40nm Technology is approximately 500nW/MFLOP resulting in 1 W power consumption

- If we linearly scale to 100 Gb/s we need 300W. We have not calculated that higher bandwidth efficiency requires higher computing performance!

- But we expect higher energy efficiency if we go to 28 nm or even 16nm scaling

Thus we need new algorithms that significantly reduce the complexity and increase the power efficiency
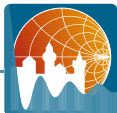
Digital Signal Processing" versus "Analog Signal Processing

Analog Case:

- Mörz et.al. published 2007 results of an analog Viterbi Decoder for FEC with 800Mb/s @120mW in a 0.25µm SiGe technology i.e. 0,16 nW/(b/s)

- They predicted that a potential of 0,06 nW/(b/s) can be achieve using that approach.
  The energy efficiency as apposed to the digital solution is 50 times higher than the digital solution at 40nm

- Taking scaling into account the energy efficiency of the analog solution is at least 100 times higher than the equivalent digital one

- Not all algorithms that work for DSP also work for analog signal processing

Thus we have to search for algorithms that fit to analog realization

Protocol Design Challenges

- To achieve 100Gb/s with a MAC processor for a wireless system we need to go to very long data packets to reduce overheads

- Long data packets need interim re-synchronization

- Since the residual error rate of a wireless system is at least 10^{-5} higher than that of a wired system most effort need to be spend in a balance between FEC and ARQ (Automatic Repeat Request)

- ARQ need to store the packets thus the memory requirement to store not acknowledged packet will be huge

- The transmission bandwidth of current computers (PCIe 2.0) is for all 16 lane approximately 120 Gb/s. With PCIe 3.0 it will be 180-200 Gb/s

- Even if this is going to much higher in the future we need to find new trade-offs between the network processor, other processor like the GPU the memory access and the main processor to balance the bus load

## List of SPP1655 Projects   1 of 2

- **LP100** – Optimizing 100Gb/s short range radio systems under energy constraints

- **SPARS** – Development of Novel System and Component Architectures for Future Innovative 100 GBit/s Communication Systems

- **Tera50** – A Radio measurement system for frequencies of 10 GHz to 1000 GHz with 50 GHz bandwidth

- **DAAB** – On-Chip Integrated Distributed Amplifier and Antenna Systems in Locally-Backside-Etched SiGe BiCMOS for Receivers with Ultra-Large Bandwidth

- **maximumMIMO** – Maximal spectral efficiency by parallel MIMO transmission using 3D antenna topologies

List of SPP1655 Projects   2 of 2

- **M4** – Ultra Wideband Communications based on Massive MIMO and Multi-mode Antennas Suitable for Mobile Handheld Devices

- **DataRace** – Integrated active group antenna including polarization multiplexing for broadband communication in W-Band

- **Real100G.COM** – Mixed-Mode Baseband for 100 Gbit/s Wireless Communication

- **Real100G.RF** – Integrated Radio-Frontend module for wireless 100Gbps communications

- **End2End100** – Network interface card for protocol processing of wireless 100 Gbps communication systems
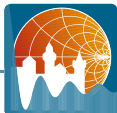
Conclusion

- Wireless 100Gb/s is still a challenge
- Several different approaches can be chosen for different scenarios of application
- The power consumption caused by system inefficiencies needs to be solved
- There seems to be a chance for a reconsideration of doing signal processing in the analog domain due to extreme high power-efficiency for certain forms of calculation

- The project started in 2013 and results have been presented (also here on EUROCON)
- Second phase started in October 2016

- Acknowledgement:
- Thanks to DFG for supporting the activities in SPP1655
- Thanks to all colleagues working within SPP1655 for leaving me several slides and pictures for use in this talk

Further Information

- SPP1655 homepage: www.wireless100gb.de

Thank you for your attention!